Flat Panel Display: Principle and Driving Circuit Design

Chapter 4
Driving Circuit Design of A-Si TFT

Outline

Ch4. Driving Circuits Design of A-Si TFT

– Gate Driving Circuit
– Source Driving Circuit
– LCD-TV Driving Technology
– Small-Size TFT-LCD Driver IC
– Trends of Digital Interface

Introduction to LCD Driver IC

• Improved Visualization:
  – A Fundamental Market Enabler

Driving Circuits of TFT-LCD Module
Driving Circuits of TFT-LCD Module

• Example

Gate Driver IC

• Also called scan driver or row driver

• Function
  – Read in start signal
  – Progressively turn on pixel TFTs on each gate line
  – Turn off TFT during pixel holding period

• Design consideration
  – RC delay of bus line (for large-size panel)

• Capacitive coupling driving (CC driving)

• Gate-driver in panel

Gate Driver Architecture

Bi-directional Shift Register

Level Shifter

Output Buffer

To Display Area

S/R frequency: 10kHz~75kHz, Output voltage range: > 12V

Gate driver IC 電路方塊圖

Timing of Gate Driver

CLK

StP

Gate driver 1

Gate driver 2

256 CLK

Gate driver 1

Gate driver 2
**Key Specifications**

- Channel number (240, 256, 264, 270, 300, 308…)
- Max. operation frequency (200KHz, 500KHz)
- 2 level or 3 level driving
- Operation voltage
  - digital: 5V, 3.3V
  - analog: VGG>20V, VEE<-10V
- Package (TCP, COG, COF)

**Package of Driver IC**

![Package Diagram](image)

The diagram shows the components of the driver IC package, including:

- **Board (Chip-On-Glass):**
  - Tstorage: -30°C to +85°C
  - Vibration Durability: 2.9 G

- **Driver LSI Chip:**
  - ACF-CDG: Anisotropic Conductive Film-Chip On Glass

- **ACF (Anisotropic Conducting Film):**
  - Bonds LSI Chip to Panel Electrode

- **Conductive Particles:**

**Source:**

- Chart showing percentage data for TCP, COG, and COF over the years 2001 to 2006.
Channel Number vs. Resolution

- **Gate driver**: No. of driver and No. of output channel

<table>
<thead>
<tr>
<th>lines</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
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<tbody>
<tr>
<td>VGA</td>
<td>480</td>
<td>120</td>
<td></td>
<td></td>
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<tr>
<td>SVG</td>
<td>600</td>
<td>120</td>
<td>150</td>
<td>200</td>
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<td>XGA</td>
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<td>SXGA</td>
<td>1024</td>
<td>256</td>
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<tr>
<td>UXGA</td>
<td>1200</td>
<td>240</td>
<td>300</td>
<td></td>
</tr>
</tbody>
</table>

Power On/Off Sequence

This IC is a high-voltage LCD driver, so it may be damaged by a large current flow if an incorrect power sequence is used. Connecting the drive powers, VEE & VGG, after the logical power, VDD, is the recommended sequence.

Gate Driver Circuits

Example

| Shift register | Level shifter | Buffer |

CMOS Shift Register

Static S/R
Shift Register

- **Latch**
  - Basic memory element
  - Two cross-coupled logic inverter
  - Bistable circuit

Shift Register – Latch 1

Level Shifter – Example 1

Inverter Type

- With both transistors of the inverters turned on, a current path from the supply voltage to ground is present, resulting in **undesirable power consumption**.

Ref: Low Power Digital VLSI Design, A. Bellaouar, M. Elmasry
Level Shifter – Example 2

This circuit overcomes the problem of direct power consumption by using a latch.

Latch Type

Output Buffer

Area ratio = e (2.7) ~ 3

TSMC HV Process

<table>
<thead>
<tr>
<th>High Voltage Characteristics</th>
<th>0.35-micron</th>
<th>0.25-micron</th>
<th>0.18-micron</th>
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<tbody>
<tr>
<td>Technology</td>
<td>1-2P4M</td>
<td>1P5M</td>
<td>1P6M</td>
</tr>
<tr>
<td>HV / LV</td>
<td>12V / 3.3V</td>
<td>18V / 3.3V</td>
<td>40V / 3.3V</td>
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<tr>
<td>HV device structure</td>
<td>DDD</td>
<td>DDD</td>
<td>LD MOS</td>
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<td>Well</td>
<td>Twin Well</td>
<td>Twin Well</td>
<td>Quad Well</td>
</tr>
<tr>
<td>Isolation</td>
<td>LOCOS</td>
<td>STI</td>
<td></td>
</tr>
<tr>
<td>Capacitor type</td>
<td>PIP</td>
<td>MIM</td>
<td></td>
</tr>
<tr>
<td>Idsat_N+HV (nA/μm)</td>
<td>400 / 250</td>
<td>260 / 170</td>
<td>400 / 230</td>
</tr>
<tr>
<td>Major Application</td>
<td>LCD Source Driver</td>
<td>LCD Gate Drive Power IC</td>
<td>One Chip Small Panel LCD Driver</td>
</tr>
<tr>
<td>Logic Compatible</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Roadmap of High Voltage Technology

- Roadmap of TSMC HV technology

Source: Web of TSMC
Two-Line Scanning

- Frame inversion
- Column inversion
- Row inversion
- Dot inversion

Two-Line Scanning

- First pulse is for precharge

Scan Driver Consideration

Dual Driving

Gate Driver Design

Toshiba 15” UXGA

Shut circuit was inserted between S/R outputs and L/S inputs to avoid overcurrent phenomena due to timing differences between right and left side scan driver outputs.

Level shifter is divided into two stages. First stage is made to shift high level from 10 V to 15 V, second stage is made to shift low level from 0 V to -2 V.
Three-level Capacitive Coupling Driving (C. C. Driving)

- Cst on gate

\[ \Delta V_1 = \Delta V_2 + \Delta V_3 \]

Pixel voltage

\[ \Delta V2 = V_{gcl} \times \frac{C_{gd}}{C_{st} + C_{gd} + C_{ds}} \]

\[ \Delta V3 = V_{gc} \times \frac{C_{gd}}{C_{st} + C_{gd} + C_{ds}} \]

If \( \Delta V_1 = \Delta V_2 + \Delta V_3 \) i.e. \( V_{gcl} \times C_{gd} = V_{gc} \times (C_{st} + C_{gd}) \)

\[ V_{gc} = V_{gcl} \times \frac{C_{gd}}{C_{st} + C_{gd}} \]

- Feed-through effect is eliminated.

Three-level C. C. Driving

Cs on Gate with 3-Level Driving Scheme

Data Line Voltage Level

Positive Driving

Negative Driving

Black(+)

White(+)

Black(-)

White(-)

Temporal Pixel Voltage Level

Positive Driving

Final Pixel Voltage Level

Scan line n

Scan line n-1

\[ V_{com} \]

\[ V_{gcl} \]

\[ V_{gc} \]

Black(+)

White(+)

Black(-)

White(-)

Not valid for Vcom AC

Four-level C. C. Driving

Cs on gate

Scan line n-1

Scan line n

\[ V_{gcl} \]

\[ V_{gc} \]

\[ V_{black} \]

\[ V_{p} \]

\[ V_{com} \]

\[ V_{e+} \]

\[ V_{e-} \]

\[ V_{gs(+)} \]

\[ V_{gs(-)} \]

\[ V_{gs(+)} \]

\[ V_{gs(-)} \]

Negative Polarity

Positive Polarity

• Line inversion

• Low voltage source driver

• Complex scan driver
Four-level C. C. Driving

\[ \Delta V_1 = \frac{V_{g} + (V_{e})}{C_{st} + C_{ic} + C_{gd}} \times C_{gd} \]
\[ \Delta V_2 = \frac{V_{e}}{C_{st} + C_{ic} + C_{gd}} \times C_{st} \]
\[ \Delta V_3 = \frac{V_{e} - (V_{e})}{C_{st} + C_{ic} + C_{gd}} \times C_{gd} \]
\[ \Delta V_4 = \frac{V_{g} - (V_{e} + V)_{d}}{C_{st} + C_{ic} + C_{gd}} \]
\[ \Delta V_5 = (V_{e} - (V_{e} + V)_{d}) \times C_{st} \]
\[ \Delta V_6 = (V_{e} + V)_{d} \times C_{gd} \]

\[ \therefore \Delta V_1 + \Delta V_2 - \Delta V_3 = -\Delta V_4 + \Delta V_5 - \Delta V_6 \]
\[ \therefore (V_{e} - (V_{e} + V)_{d}) = 2V_{g} \times \frac{C_{gd}}{C_{st}} \]

- Pixel voltages of positive polarity and negative polarity for LC cell are symmetry.

Comparison of Addressing

<table>
<thead>
<tr>
<th>Frame Common voltage</th>
<th>Row Low/high voltage</th>
<th>Column Voltage Level</th>
<th>Dot Voltage Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-level driving V</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>3-level driving X / V</td>
<td>X / V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>4-level driving X / V</td>
<td>X / V</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Frame Common voltage</th>
<th>Row Low/high voltage</th>
<th>Column Voltage Level</th>
<th>Dot Voltage Level</th>
</tr>
</thead>
<tbody>
<tr>
<td>2-level driving V</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>3-level driving X / V</td>
<td>X / V</td>
<td>V</td>
<td>V</td>
</tr>
<tr>
<td>4-level driving X / V</td>
<td>X / V</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

Trend of Gate Driver IC

- package:
  - TCP (Tape Carrier Package) →
  - COG (Chip on Glass) →
  - COF (Chip on Film) →
  - GIP (Gate-Driver In Panel) →
Ch4. Driving Circuits Design of A-Si TFT

- Gate Driving Circuit
- Source Driving Circuit
  - Driver Architectures
  - Driver Specifications
  - DAC
  - Output Buffer
  - Low power consumption
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface

Source Driver Circuits
- Also Called Column Driver (Data Driver)
- Driver Architectures
  - Line-at a-time (LAAT)
  - Point-at a-time (PAAT)
- Data Drivers Types
  - Analog Data Driver
  - Digital Data Driver

Analog Data Driver
- Serial In, Serial Out
  - Shift Register
  - Video in
  - Qi
  - Qi+1
  - Pixel
  - Shorter charging time
- Serial In, Parallel Out
  - Shift Register
  - Video in
  - Qi-1
  - Qi
  - Qi+1
  - Qi+2
  - Sample capacitor
  - Control
  - Hold capacitor
  - Pixel
### Comparison of Analog Data Driver

<table>
<thead>
<tr>
<th></th>
<th>SISO 1 phase</th>
<th>SIPO 1 phase</th>
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</thead>
<tbody>
<tr>
<td>Circuits complexity</td>
<td>lowest</td>
<td>higher</td>
</tr>
<tr>
<td>Pixel charging time</td>
<td>$T_{VL}/P_x$</td>
<td>$T_{VL}$</td>
</tr>
<tr>
<td>Sample time</td>
<td>$T_{VL}/P_x$</td>
<td>$T_{VL}/P_x$</td>
</tr>
<tr>
<td>S/R frequency</td>
<td>$1/(T_{VL}/P_x)$</td>
<td>$1/(T_{VL}/P_x)$</td>
</tr>
<tr>
<td>Reformed video needed</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>

TVL: vertical line time, P_x: horizontal pixel number

### LAAT Driver Architecture

For a-Si TFT-LCDs

- CLK, DIO
- Video in
- Driver IC
- Array

- All video signals stored in A latches are written to B latches simultaneously in each horizontal scanning period. Features: (1) has sufficient charging capability; (2) very difficult to achieve good uniformity of output voltages of the analog buffer.

### PAAT Driver Architecture

For some large-size LTPS TFT-LCDs

- CLK, DIO
- Video in
- Driver
- Array

A high speed and wide voltage range analog interface circuit that consumes a large amount of power is required!! Feature: (1) less data driver ICs; (2) shorter pixel charging time than LAAT.

### LAAT vs. PAAT

<table>
<thead>
<tr>
<th>Units</th>
<th>Size</th>
<th>Resolution</th>
<th>Frequency</th>
<th>Technique</th>
<th>Multiplex</th>
<th>Gray Scale Bits</th>
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<tbody>
<tr>
<td></td>
<td>Inches</td>
<td></td>
<td>MHz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fujitsu</td>
<td>3.2</td>
<td>XGA</td>
<td>6.3</td>
<td>LAAT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LG</td>
<td>4</td>
<td>800x600</td>
<td>2.5</td>
<td>PAAT</td>
<td>LAAT</td>
<td>8</td>
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<tr>
<td>Mitsubishi</td>
<td>3.5</td>
<td>640x480</td>
<td>12.5</td>
<td>PAAT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sharp</td>
<td>3.7</td>
<td>1280x720</td>
<td>6.5</td>
<td>PAAT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sharp</td>
<td>2.2</td>
<td>640x480</td>
<td>2.4</td>
<td>LAAT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sharp</td>
<td>3.7</td>
<td>720x480</td>
<td>3.15</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sharp</td>
<td>2.6&quot;</td>
<td>720x480</td>
<td>13.8</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Sanyo has been selling products using the PAAT technology. Since small-size panels have only 234 scan line, there is sufficient time to use PAAT technology.
- Seiko-Epson has adopted the LAAT architecture because the studies indicated that the crosstalk on a multiplexed circuit was too severe.
Max. Frequency of Shift Registers

\[ V_{cc} = 5V, \text{Freq.} < 2 \text{MHz} @ \mu n/p = 70/35 \text{ cm}^2/\text{Vs} \]

Ref: SID’96 Digest, pp.673.

Digital Data Driver

(a) Decoder type is very difficult to achieve full gray scale because the circuit configuration is too complicated.

(b) DAC type is the most promising one because it has a less complicated configuration while keeping full digital interface.

Ref: IDW 00’ p.171

Comparison of Digital/Analog Data Driver

<table>
<thead>
<tr>
<th></th>
<th>Digital</th>
<th>Analog</th>
</tr>
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<tbody>
<tr>
<td>circuits complexity</td>
<td>complex</td>
<td>simple</td>
</tr>
<tr>
<td>noise immunity</td>
<td>high</td>
<td>low</td>
</tr>
<tr>
<td>gamma correction</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>video signal processing</td>
<td>Compatible to PC</td>
<td>ADC needed</td>
</tr>
<tr>
<td>cost</td>
<td>high</td>
<td>low</td>
</tr>
</tbody>
</table>

Ref: SID’96 Digest, pp.673.

Architecture of Source Driver IC for Large-Size TFT-LCDs

Digital/Analog Converter, DAC

Output buffers

Level Shifter

Digital Part

Analog Part

To LCD data line
### Timing Diagram of Source Driver

- **CLK**
- **DIO1**
- **DIO2**

Data latch:

- 1st 384 Outputs for 1~128 Pixel
- 2nd 384 Outputs for 129~256 Pixel

---

### Key Specifications

- Channel number (384, 402, 420, 480, 640, 720…)
- Gray scale (6 bit, 8 bit, 10 bit…)
- Max operation frequency (45MHz, 55MHz, 65MHz, 75MHz…)
- Pixel charging time (eg. R=2k, C=20pF, 6.5us 90%, 11.5us 99.9%)  
- Frame/row/column/dot inversion
- Output voltage deviation (±20mV, ±10mV, ±5mV, ±3mV)
- Output voltage (10V, 12V, 15V, 18V)
- Interface (TTL, RSDS, mini-LVDS)
- Operation voltage (2.5V, 3.3V)
- No. of Gamma reference voltage (10, 14, 18)
- Package (TCP, COG, COF)
- Others (data inversion, low-power mode, offset canceling, charge sharing …etc.)

---

### Channel Number vs. Resolution

<table>
<thead>
<tr>
<th>Source driver</th>
<th>No. of lines</th>
<th>12</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
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</thead>
<tbody>
<tr>
<td>VGA</td>
<td>640x3</td>
<td>192</td>
<td>240</td>
<td></td>
<td></td>
<td></td>
<td>384</td>
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<tr>
<td>SVGA</td>
<td>800x3</td>
<td>240</td>
<td>300</td>
<td></td>
<td></td>
<td>402</td>
<td>480</td>
<td></td>
</tr>
<tr>
<td>XGA</td>
<td>1024x3</td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td>384</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SXGA,WXGA</td>
<td>1280x3</td>
<td></td>
<td></td>
<td>384</td>
<td></td>
<td>480</td>
<td>640</td>
<td></td>
</tr>
<tr>
<td>WXGA</td>
<td>1366x3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>414</td>
<td></td>
<td></td>
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<tr>
<td>SXGA+</td>
<td>1400x3</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>420</td>
<td></td>
<td></td>
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<tr>
<td>WXGA+</td>
<td>1440x3</td>
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<td>432</td>
<td>480</td>
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<td>UXGA</td>
<td>1600x3</td>
<td>402</td>
<td>480</td>
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<tr>
<td>WSXGA+</td>
<td>1680x3</td>
<td>420</td>
<td></td>
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<td></td>
<td>720</td>
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<td>1920x3</td>
<td>642</td>
<td>720</td>
<td></td>
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<tr>
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<td>512</td>
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### Resolution vs. Max. Frequency

<table>
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<tr>
<th>Frame rate</th>
<th>60 Hz</th>
<th>60 Hz</th>
<th>75 Hz</th>
<th>75 Hz</th>
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<tr>
<td></td>
<td>Pixel frequency</td>
<td>Horizontal period</td>
<td>Pixel frequency</td>
<td>Horizontal period</td>
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<tr>
<td>VGA</td>
<td>25.2 MHz</td>
<td>31.7 μs</td>
<td>31.5 MHz</td>
<td>26.7 μs</td>
</tr>
<tr>
<td>SVGA</td>
<td>40 MHz</td>
<td>26.4 μs</td>
<td>49.5 MHz</td>
<td>21.3 μs</td>
</tr>
<tr>
<td>XGA</td>
<td>65 MHz</td>
<td>20.7 μs</td>
<td>78.75 MHz</td>
<td>16.7 μs</td>
</tr>
<tr>
<td>SXGA</td>
<td>108 MHz</td>
<td>15.6 μs</td>
<td>135 MHz</td>
<td>12.5 μs</td>
</tr>
<tr>
<td>UXGA</td>
<td>162 MHz</td>
<td>13.3 μs</td>
<td>202.5 MHz</td>
<td>10.7 μs</td>
</tr>
</tbody>
</table>

Higher resolution, shorter pixel charging time, higher driving frequency.

### D/A Converter

- Fundamentals of Data Converter
- Digital-to-Analog Converters

### Fundamentals of Data Converter

- Ideal D/A converter
- Quantization error in ideal DACs
- Performance limitation
- Offset error
- Gain error
- Accuracy

### Idea D/A Converter

- Ideal N-bit DAC
  
  ![Digital input formula](image)

  Where \(b_i\) is 1 or 0, i.e. binary, \(b_{n-1}\) is the MSB, and \(b_0\) is the LSB

  Digital input

  \[B_{in} = \frac{b_{n-1}}{2^1} + \frac{b_{n-2}}{2^2} + L \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\]

  Analog output

  \[V_{out} = V_{Ref} \times B_{in}\]

  Analog reference \(V_{Ref}\)
Idea D/A Converter (cont')

- Analog output $V_{out}$ is related to $B_{in}$ through an analog reference, $V_{Ref}$.
  1. $V_{out}$ and $V_{Ref}$ may be voltage, current, or charge.
  2. We assume here that they are voltage (for simplicity).
  3. Definitions:

\[
V_{out} = V_{ref} \left( \frac{b_{n-1}}{2^1} + \frac{b_{n-2}}{2^2} + \cdots + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n} \right) = V_{ref} \times B_{in},
\]

\[
V_{LSB} = \frac{V_{ref}}{2^N}, \quad \text{where } V_{LSB} \text{ is defined as the voltage changes when one LSB changes.}
\]

- 1 LSB = $1/2^N$ unitless definition.

Quantization Error in DACs

- **Quantization error** (noise) is the inherent uncertainty in digitizing an analog value with a finite resolution converter. It is equal to the analog output of the infinite-bit DAC minus that of the finite-bit DAC.

Performance Limitation

- Definitions for determining the transfer responses for DACs.
  - The transfer response of a DAC is defined to be the analog levels that occur for each of the digital word.
  - Resolution
    - The number of distinct analog levels corresponding to different digital words. Thus, an $N$-bit resolution implies that the converter can resolve $2^N$ distinct analog levels.
### Offset Error

- Offset error is in units of LSBs.
- Offset error is the output that occurs for the input code that should produce zero output.

\[ E_{off}(DAC) = \frac{V_{out}}{V_{LSB}} \mid_{0...0} \]

- **2-bit example**: 
  
  ![Diagram of offset error](image)

### Gain Error

- Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero.
- Gain error is in units of LSBs.
- DACs:

\[ E_{Gain(DAC)} = \left( \frac{V_{out}}{V_{LSB}} \right)_{1...1} - \left( \frac{V_{out}}{V_{LSB}} \right)_{0...0} - (2^N - 1) \]

- **2-bit example**:

  ![Diagram of gain error](image)

### Accuracy

- **Absolute accuracy**
  - The difference between the expected and actual and transfer response.
  - Includes 1. offset error, 2. gain error, 3. linearity error
- **Relative accuracy**
  - The accuracy of offset and gain errors have been removed

### Accuracy (cont’)

- Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bit, or as a fraction of an LSB.
  - For example, a 12-bit accuracy implies that the converter’s error is less than the full-scale divided by \(2^{12}\).
  - A converter may have 12-bit resolution with only 10-bit accuracy, or 10-bit resolution with 12-bit accuracy.
  - An accuracy greater than the resolution means that the converter’s transfer response is very precisely controlled. (better than the number of bits of resolution)
D/A Converter

- Fundamentals of Data Converter
- Digital-to-Analog Converters

Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC
- Binary-weighted converters
- Glitches
- Thermometer-code DACs

Nyquist-rate D/A converters

- Four main types
  - Decoder-based
  - Binary-weighted
  - Thermometer-code
  - Hybrid

Decoder-Based DAC

- Most straightforward approach
  - Create $2^N$ reference signals and pass the appropriate signal to the output.
- Three main types:
  - Resistor string
  - Folded resistor-string
  - Multiple resistor-string
Decoder-Based DAC

- Most straightforward approach
  - Create \(2^N\) reference signals and pass the appropriate signal to the output.
- Types:
  - **Resistor string**
  - Folded resistor-string

Resistor-string DAC

- Example 1: a 3-bit DAC with transmission gate, tree-like decoder.
- Transmission gates might be used rather than n-channel switches.
- Extra drain and source capacitance (to GND) is offset by the reduced switch resistance.
- Larger layout
- Can operate closer to positive supply voltage.

Resistor-string DAC (cont’)

- Only n-channel switches are used
  - 1. About the same speed as the transmission gate implementation.
  - 2. Compact layout (no contacts are required in the tree)
- Monotonicity is guaranteed (if the buffer’s offset does not depend on its input voltage)
- The accuracy of this DAC depends on the type of resistor used. Polysilicon (20-30 \(\Omega/\square\)) can have up to 10 bits of accuracy.

Resistor-string DAC (cont’)

- Speed
  - Can be estimated using open-circuit time-constant approach (refer to microelectronics textbook written by Sedra and Smith)
  - Time-constant
    \[
    \approx 3R_{tr}C_{tr} + 2 \cdot 3R_{tr}C_{tr} + \cdots + N \cdot 3R_{tr}C_{tr}
    \]
    \[
    = N(N+1)/(2 \cdot 3R_{tr}C_{tr})
    \]
  - Where \(R_{tr}\) is the resistance of switches, \(C_{tr}\) is drain or source capacitance of switches, and \(N\) is the bit number.
**Resistor-string DAC (cont’)**

- **Example 2**: a 3-bit DAC with digital decoding.
  - □ Compared to example 1:
    1. Higher speed
    2. More area for decoding circuit
  - □ Speed
    - Time-constant \( \approx R_{tr} \cdot 2^N C_{tr} \)
    - For \( N \leq 6 \), example 2 is faster
    - For \( N > 7 \), example 1 is faster
  - ▸ Compromise between example 1 and example 2.
    - Folded resistor-string DAC

**Decoder-Based DAC**

- Most straight forward approach
  - Create \( 2^N \) reference signals and pass the appropriate signal to the output.

- Types:
  - Resistor string
  - *Folded resistor-string*

**Folded resistor-string DAC**

- Reduced the amount of digital decoding
- Reduce large capacitive loading
- Decoding is very similar to that for a digital memory
- Example:
  - 4 bit (2 bit + 2 bit) DAC
  - Time constant \( \approx R_{tr} (2^2 C_{tr}) + 2R_{tr} (2^2 C_{tr}) \)
- Other design examples:
  - 12 bit = 6 bit + 6 bit, or 4 bit + 4 bit + 4 bit, or ……
  - 10 bit = 5 bit + 5 bit, or 3 bit + 3 bit + 4 bit, or ……
Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC

**Binary-weighted converters**

- Glitches
- Thermometer-code DACs

### Binary-Weighted (or Binary-Scaled) Converter

- An appropriate set of signals that are all related in a binary fashion
- The binary array of signals might be voltages, charges, or currents.
- Five main types:
  - Binary-weighted resistor DAC
  - Reduced-resistor-ratio ladders
  - R-2R-based DAC
  - Charge-redistribution switched-capacitor DAC
  - Current-mode DAC

**Binary-Weighted Resistor DAC**

- Does not require many resistors or switches.
- Disadvantage
  1. Resistor ratio and current ratio are on the order of 2^N. If N is large, this large current ratio requires that the switches also be scaled so that equal voltage drops appear them.
  2. Monotonicity is no guaranteed.
  3. Prone to glitch.

\[
V_{out} = -R_F V_{ref} \left( -\frac{b_3}{2R} - \frac{b_2}{4R} - \frac{b_1}{8R} \right) = \left( \frac{R_F}{R} \right) V_{ref} B_{in}
\]

\[
where: B_{in} = b_3 2^{-1} + b_2 2^{-2} + b_1 2^{-3} + \cdots
\]
Reduced-resistor-ratio Ladders

- Reduce the large resistor ratios in a binary-weighted array
- Introduce a series resistor to scale signals in portions of the array
  - Ex: $V_A = -1/4V_{\text{Ref}}$

![Diagram of Reduced-resistor-ratio Ladders]

Reduced-resistor-ratio Ladders (cont’)

- An additional 4R was added such that resistance seen to right of the 3R equals R.
- One-fourth the resistance ratio compared to the binary-weighted case.
- Current ratio has remained unchanged
  - Switches must be scaled in size.
- Repeating this procedure recursively, one can obtain an R-2R ladder.

R-2R-based DAC

- Smaller size and better accuracy than a binary-sized approach
  - Small number of components
  - Resistance ratio of only 2
- 4-bit example: $I_R = \frac{V_{\text{ref}}}{2R}$, and $V_{\text{out}} = R_F \cdot \sum_{i=1}^{N} b_i \cdot I_R = R_F \cdot \left( \frac{R_F}{R} \right) \sum_{i=1}^{N} b_i \cdot 2^{i-1}$
- Current ratio is still large → large ratio of switch sizes

![Diagram of R-2R-based DAC]

R-2R-based DAC (cont’)

- R-2R ladder DAC with equal currents through switches
- Slower since the internal nodes exhibit some voltage swings (as opposed to the previous configuration where internal nodes all remain at fixed voltage).
**Charge-redistribution switched-capacitor DAC**

- Insensitive to Op Amp input-offset voltage, 1/f noise, and finite amplifier gain.
- An additional sign bit can be realized by interchanging the clock phases (shown in parentheses).

**Current-mode DAC**

- High-speed
- Switch current to output or to ground
- The output current is converted to a voltage through $R_F$.
- The upper portion of current source always remains at ground potential.

**Digital-to-Analog Converters**

- Nyquist-rate D/A converters
- Decoder-based DAC
- Binary-weighted converters
- **Glitches**
- Thermometer-code DACs

**Glitches**

- A major limitation during high-speed operation
- Mainly the result of different delays occurring when switching different signals
- Example: $01111…1 \rightarrow 1000…0$
  1. $I_1$ represents the MSB current and $I_2$ represents the sum of $(N-1)$ LSB currents.
  2. The MSB current turns off slightly early, causing a glitch of zero current.
Glitches (cont’)

- Glitch disturbance can be reduced by:
  1. Limiting the bandwidth (placing a capacitor across RF)
  2. Using a sample and hold on the output signal.
  3. Modifying some or all of the digital word from a binary code to a thermometer code.

Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC
- Binary-weighted converters
- Glitches

- *Thermometer-code DACs*

Thermometer-Code DAC

- Digital recode the input to a thermometer-code equivalent.

<table>
<thead>
<tr>
<th>Decimal</th>
<th>Binary</th>
<th>Thermometer Codes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>b₀ b₁ b₂</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0 0 0</td>
<td>0 0 0 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1</td>
<td>0 0 1</td>
<td>0 0 0 0 0 0 0 0 0 1</td>
</tr>
<tr>
<td>2</td>
<td>0 1 0</td>
<td>0 0 0 0 0 0 0 0 0 1</td>
</tr>
<tr>
<td>3</td>
<td>0 1 1</td>
<td>0 0 0 0 0 0 0 0 1 1</td>
</tr>
<tr>
<td>4</td>
<td>1 0 0</td>
<td>0 0 0 0 0 0 0 1 1 1</td>
</tr>
<tr>
<td>5</td>
<td>1 0 1</td>
<td>0 0 0 0 0 0 1 1 1 1</td>
</tr>
<tr>
<td>6</td>
<td>1 1 0</td>
<td>0 0 0 0 0 1 1 1 1 1</td>
</tr>
<tr>
<td>7</td>
<td>1 1 1</td>
<td>0 0 0 0 1 1 1 1 1 1</td>
</tr>
</tbody>
</table>

- Advantages over its binary-weighted counterpart
  1. Low DNL errors
  2. Guaranteed monotonicity
  3. Reduced glitching noise
- Does not increase the size of the analog circuitry compared to a binary-weighted approach.
Thermometer-Code Current-Mode DAC

- Row and column decoders
- Inherent monotonicity
- Good DNL errors
- INL errors depend on the placement of the current sources

In high-speed applications

1. The output current feeds directly into an off-chip 50 Ω or 75 Ω resistor, rather than an output opamp.
2. Cascode current sources are used to reduce current-source variation due to voltage changes in $V_{out}$.

Examples of DAC 1


Examples of DAC 2

12-bit DAC Paper- A Novel Linear Digital-to-Analog Converter using Capacitor coupled Adder for LCD Driver ICs

Figure 1 Block diagram of the 8bit Resistor-String DAC.

Figure 2 Block diagram of the 10bit Resistor-Resistor String DAC (RR-DAC).
Examples of DAC 3

- 12 Bit Linear DAC using capacitor coupled adder

R-String DAC

R-String DAC (cont')

D/A Converter of Source Driver IC

DAC with ROM Decoder
Gamma Correction

T-V curve is non-linear.

Adjust the voltage of V1~V8 to obtain the desire transmittance.

Gamma Correction

10 Gamma Voltage

18 Gamma Voltage

10 Gamma Voltage

18 Gamma Voltage

R-String (ROM Decoder) DAC

- Advantages
  - Simple architecture
  - Low noise
  - Optimized gamma curve

- Disadvantages
  - Large area
  - Area increase rapidly as bit number increases
  - Steady current consumption in R-string

Output Buffer

Rail to rail OP-AMP

Polarity control signal

Odd Output

Gamma Voltage (+)

DAC P

To data line

Even Output

Gamma Voltage (-)

DAC N
Positive and negative signals are applied by DAC1 and DAC2 separately. Dynamic range of each DAC is reduced to ½ compared with conventional ones.

Reference:
Model for a Nonideal Op-Amp

- Finite differential-input impedance $R_{id}$, $C_{id}$
- Output resistance $R_{out}$
- Common-mode input resistance $R_{icm}$
- Input offset voltage $V_{os}$
- Input offset current $I_{os}=|I_{B1}-I_{B2}|$
- Common-mode rejection ratio $\frac{V_1}{CMRR}$
- Noise $i_n^2$, $e_n^2$

\[ V_{out}(s) = \frac{A_v(s)[v_1(s)-V_2(s)]}{2} + \frac{A_c(s)[v_1(s)+V_2(s)]}{2} \]


Classification of Op-Amp

<table>
<thead>
<tr>
<th>conversion</th>
<th>Hierarchy</th>
</tr>
</thead>
<tbody>
<tr>
<td>voltage to current</td>
<td>Classic differential amplifier</td>
</tr>
<tr>
<td>Current to voltage</td>
<td>Modified differential amplifier</td>
</tr>
<tr>
<td>Current to voltage</td>
<td>Differential-to-single-ended load</td>
</tr>
<tr>
<td>Current load</td>
<td>Source/sink Current load</td>
</tr>
<tr>
<td>MOS diode load</td>
<td>Transconductance grounded gate</td>
</tr>
<tr>
<td>Transconductance</td>
<td>Grounded gate</td>
</tr>
<tr>
<td>Class A</td>
<td>Class B (push-pull)</td>
</tr>
</tbody>
</table>


Examples of Op-Amp

- Classical two-stage CMOS op amp
- Folded-cascode op amp


Design of Op Amp

- Procedures
  - Choosing or creating the basic structure
  - Select dc currents and transistor size
  - Boundary conditions
    - Process specification ($V_t$, $k'$, $C_{ox}$…)
    - Supply voltage/current and range
    - Operating temperature and range

Design of Op Amp

- Performance requirement
  - Gain
  - Gain bandwidth
  - Settling time
  - Slew rate
  - Input common-mode range, ICMR
  - Common-mode rejection ratio, CMRR
  - Power-supply rejection ratio, PSRR
  - Output voltage swing
  - Output resistance
  - Offset
  - Noise
  - Layout area

Example
- \( \geq 70 \text{ db} \)
- \( \leq 5 \text{ MHz} \)
- \( \leq 1 \text{ us} \)
- \( \leq 5 \text{ V/us} \)
- \( \leq 1.5 \text{ V} \)
- \( \geq 60 \text{ db} \)
- \( \leq 60 \text{ db} \)
- \( \leq 1.5 \text{ V} \)
- N/A
- \( \leq 10 \text{ mV} \)
- \( \leq 100 \text{ nV/} \sqrt{\text{Hz}} @ 1 \text{ kHz} \)
- \( \leq 5000 \times (\text{min. L})^2 \)

Model Parameters for a Typical CMOS Bulk Process

<table>
<thead>
<tr>
<th>Parameter symbol</th>
<th>Process description</th>
<th>Typical parameter value</th>
<th>unit</th>
</tr>
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<tbody>
<tr>
<td>( V_{T0} )</td>
<td>Threshold voltage (( V_{BS}=0 ))</td>
<td>0.7±0.15</td>
<td>-0.7±0.15</td>
</tr>
<tr>
<td>( K' )</td>
<td>Transconductance parameter (in sat.)</td>
<td>110.0±10%</td>
<td>50.0±10%</td>
</tr>
<tr>
<td>( \gamma )</td>
<td>Bulk threshold parameter</td>
<td>0.4</td>
<td>0.57</td>
</tr>
<tr>
<td>( \lambda )</td>
<td>Channel length modulation parameter</td>
<td>0.04(L=1um)</td>
<td>0.05(L=1um)</td>
</tr>
<tr>
<td>( 2</td>
<td>\phi F</td>
<td>) Surface potential at strong inversion</td>
<td>0.7</td>
</tr>
</tbody>
</table>


Design of Op Amp

- Procedures
  - Decide on a suitable configuration
    - Trade-off between noise, offset, power...
  - Determine the compensation method
    - Especially for very large \( C_{LOAD} \)
  - Design device sizes for proper dc, ac, and transient performance
    - Hand calculation: 80% → important to get a feel for sensitivity of parameter variation
    - Computer simulation: 20% → for optimization

Rule: (use of simulator) x (common sense) = constant

Model parameters for a typical CMOS bulk process using the simple model with values based on a 0.8um silicon-gate bulk CMOS n-well


Model Parameters for a Typical CMOS Bulk Process

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Frequency and Phase Response (1/3)

- For a single-loop, negative-feedback system

Stable \( \Rightarrow |A(j \omega_0) F(j \omega_0)| = |L(j \omega_0)| < 1 \)

where \( \omega_0 \) is defined as \( \text{Arg}[A(j \omega_0) F(j \omega_0)] = \text{Arg}[L(j \omega_0)] = 0^\circ \)

or \( \text{Arg}[A(j \omega_{0dB}) F(j \omega_{0dB})] = \text{Arg}[L(j \omega_{0dB})] > 0^\circ \)

where \( \omega_{0dB} \) is defined as \( |A(j \omega_{0dB}) F(j \omega_{0dB})| = |L(j \omega_{0dB})| = 1 \)


Display Tech. & Circuit Design Lab. 98(上) NCHU / EE /汪芳興 fansen@dragon.nchu.edu.tw

Frequency and Phase Response (2/3)

• Bode Plots:
  - \(|A(j\omega) F(j\omega)|\) & \(\text{Arg}[- A(j\omega) F(j\omega)]\)

Phase Margin
\(\Phi_M = \text{Arg}[L(j\omega_{0dB})]\)


Frequency and Phase Response (3/3)

• Time response of a second-order system
  - Large P.M. results in less ‘ringing’ → good stability
  - P.M. >45° (at least), > 60° (preferable)


Second-order Uncompensated Op Amp

• Small-Signal Equivalent Circuit

\(P'_1 = -1/(R_1C_1)\)
\(P'_2 = -1/(R_{II}C_{II})\)
If \(F(s)=1\) (worst case)
PM <= 45°
→ need compensation


Miller Compensation of Op Amp

• Miller Compensation Technique

\(P_1 = -1/(g_{mII}R_II R_{II}C_C)\)
\(P_2 = -g_{mII}C_C/(C_{II}C_{II}+C_{II}C_C+C_{II}C)\) \(\approx -g_{mII}/C_{II}\)
\(Z_1 = g_{mII}/C_C\)

Miller Compensation of Op Amp

- Root locus plot of the loop gain $F(s)=1$
- Bode plots
  - $P_2$ does not affect the magnitude until after $|AF|<1$
  - $Z_1$ increases the phase shift

Bode plots


Two Stage Op Amp with Parasitic $C$

- There are more than two pole due to $C_1, C_2, C_3, \ldots$
- We will concentrate on two most dominant (small) pole and the RHP zero.

$$p_1 \approx \frac{-G_1G_{II}}{g_{ml}C_C} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}C_C}$$

$$p_2 \approx -\frac{g_{ml}}{C_{II}} = -\frac{g_{m6}}{C_2}$$

$$Z_1 \approx \frac{g_{ml}}{C_C} = \frac{g_{m2}}{C_C}$$

Unit gain bandwidth:

$$\text{GB} \approx \frac{g_{ml}}{C_C} = \frac{g_{m2}}{C_C}$$


Miller Compensation Technique

- $P_1$: **miller pole** and accomplish the desire compensation
- $M_6$ is a NMOS. $C_C$ is multiplied by the gain of the 2nd stage, $g_{ml}R_{II}$, to give a capacitor in parallel with $R_I$ of $g_{ml}R_{II}C_C$
- Multiplying $g_{ml}R_{II}C_C$ times $R_I$ and inverting it. Then we get

$$p_1 \approx \frac{-G_1G_{II}}{g_{ml}C_C} = \frac{-(g_{ds2} + g_{ds4})(g_{ds6} + g_{ds7})}{g_{m6}C_C}$$


Miller Compensation Technique

- $P_2$: **output pole**, at least equal to GB and is due to the capacitance at the output of the op amp.
  - $C_{II} = C_L$ (load capacitance).
  - Since $|p_2|$ is near or greater than $GB$, the reactance of $C_C$ is approximately $1/(GBC_C)$ and is very small.
  - $M6$ is a MOS diode and its small signal resistance is $g_{m6}^{-1}$.
  - Multiplying $g_{m6}^{-1}$. by $C_{II}$ and inverting gives

$$p_2 \approx -\frac{g_{ml}}{C_{II}} = -\frac{g_{m6}}{C_2}$$

Miller Compensation Technique

- \( Z_1 \) (the RHP zero) boosts the loop gain magnitude while causing the loop phase shift to become more negative. → undesirable
- It worsens the stability of the op amp.
- It comes from the two feedback paths.

- The signals through these two paths may be equal and opposite and cancel, creating the zero.

\[
V_{out}(s) = \left( -\frac{g_m R_H}{R_H + sC_C} \right) V^\prime + \left( \frac{R_H}{R_H + 1/sC_C} \right) V^\prime\prime = -\frac{R_H(\frac{g_m}{sC_C} - 1)}{R_H + 1/sC_C} V
\]

Output Deviation of Buffer

Offset Cancellation

Phase 1

- \( V_{offset} \)
- \( V_{in} \)
- \( V_{voffset} \)
- \( V_{vcaz} \)

- How Long the Ph1 is enough to sample the correct \( V_{offset} \)?
- How Long the Ph2 is enough to charge the pixel voltage?

Layout of Source Driver

384 channel source driver

420 channel source driver

480 channel source driver

Layout length/channel < 2 cm / 480 = 41 um
**TSMC HV Process**

### High Voltage Process Characteristics

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.35-micron</th>
<th>0.25-micron</th>
<th>0.18-micron</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>1P2M</td>
<td>1P4M</td>
<td>1P6M</td>
</tr>
<tr>
<td>HV/LV</td>
<td>12V/3.3V</td>
<td>18V/3.3V</td>
<td>40V/5V</td>
</tr>
<tr>
<td>HV device structure</td>
<td>DDD</td>
<td>DDD</td>
<td>LDMOS</td>
</tr>
<tr>
<td>Well</td>
<td>Twin Well</td>
<td>Twin Well</td>
<td>Quad Well</td>
</tr>
<tr>
<td>Isolation</td>
<td>LOCOS</td>
<td>STI</td>
<td></td>
</tr>
<tr>
<td>Capacitor type</td>
<td>PIP</td>
<td>MIM</td>
<td></td>
</tr>
<tr>
<td>I(d) N.P. HV (nA/µm)</td>
<td>400/250</td>
<td>260/170</td>
<td>400/230</td>
</tr>
<tr>
<td>Major Application</td>
<td>LCD Source Driver</td>
<td>LCD Gate Drive Power IC</td>
<td>One Chip Small Panel LCD Driver</td>
</tr>
<tr>
<td>Process Ready</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Logic Compatible</td>
<td>Yes</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

---

**Power Saving mode (1)**

- Start pulse input for 1st IC
- Start pulse output for 1st IC
- Clock disable signal for 1st IC
- Start pulse input for 2nd IC
- Start pulse output for 2nd IC
- Clock disable signal for 2nd IC
- Start pulse input for 8th IC
- Start pulse output for 8th IC
- Clock disable signal for 8th IC

### Turn on one clock

\[ P = f_d \times C \times \frac{dV}{dt} \]

---

### Power Saving mode (2)

**Distribute clock tree**

- Clock 1
- Clock 2

---

### Power Saving mode (3)

#### Dual edge clocking

- CK1
- XCK1
- CK2
- XCK2

\[ 6 \times 3 \times 3 \]
Charge Sharing

Because only half of the charges with positive potential are recycled, power saving efficiency of the previous charge sharing is theoretically limited to 50%.

Waveform of LCD Driver

XGA@75Hz Dot Inversion

Power Consumption of LCD Source Driver

- Large size panel: 4~8mA
- CNS for Car: 2~3mA
- DSC, Game, PDA: 0.5~2mA
- Mobile-phone: <0.3mA (power saving)
Trend of LCD Source Driver

- 6-bit / 8-bit to 10-bit resolution
- 384 / 480 to >500 output channels for SXGA+ / WSXGA+ / UXGA / WUXGA panel
- TTL to RSDS/mini-LVDS data interface for low power and EMI issue
- 10V to 18V for wide-view-angle panel
- Reduced chip size for cost down
- Low power consumption
- TV application

Outline

Ch4. Driving Circuits Design of A-Si TFT
- Gate Driving Circuit
- Source Driving Circuit
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface

LCD TV vs. LCD Monitor

<table>
<thead>
<tr>
<th>性能</th>
<th>液晶顯示器</th>
<th>液晶電視</th>
</tr>
</thead>
<tbody>
<tr>
<td>亮度</td>
<td>中亮度 (200-300 cd/m²)</td>
<td>高亮度 (400-500 cd/m²)</td>
</tr>
<tr>
<td>可見時間</td>
<td>8-16 ms (採用OD液晶加速技術)</td>
<td>3-8 ms</td>
</tr>
<tr>
<td>色域</td>
<td>72% NTSC色域 (i.e. sRGB規格)</td>
<td>90% NTSC色域</td>
</tr>
<tr>
<td>可視角度</td>
<td>120° (水平), 90° (垂直)</td>
<td>170° (水平), 170° (垂直)</td>
</tr>
<tr>
<td>視聽對象</td>
<td>電腦資料與影片</td>
<td>電視影像, DVD映像</td>
</tr>
</tbody>
</table>

表1 液晶顯示器與液晶電視的性能比較

LCD TV Electronics

LCD Control Board

<table>
<thead>
<tr>
<th>Component</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Antenna RF in</td>
<td>Tuner</td>
</tr>
<tr>
<td>Composite video YCbCr</td>
<td>Y/C</td>
</tr>
<tr>
<td>YPbPr Analog RGB Digital DVI</td>
<td>Video Decoder</td>
</tr>
<tr>
<td>TMDS Rx</td>
<td>ADC</td>
</tr>
<tr>
<td>TMDS Tx</td>
<td>Scaler</td>
</tr>
<tr>
<td>DC/DC power</td>
<td>MCU</td>
</tr>
<tr>
<td>Inverter</td>
<td>Set-Top Box</td>
</tr>
<tr>
<td>Back light unit</td>
<td></td>
</tr>
</tbody>
</table>

Display Area

- Mini-LVDS/RSDS/TTL transceiver
- HDTV: 1920x1080; 1280x720
- WXGA: 1366x768/1280x768
- SDTV: 720x480

ASIC (T-CON, RSDS/TTL transmitter)

PCB with data bus

Data driver

Set-Top Box

LCD Module

Tuner

Y/C

Video Decoder

De-interface

OSD

Scaler

ADC

Sync Sep.

TMDS Rx

TMDS Tx

TTL/LVDS/TMDS

DC/DC power

Inverter

Back light unit
**Digital TV System**

- **Digital Tuner**
- **VSB/COFDM Demodulator**
- **MPEG2 Decoder**
- **POD/CI**
- **Scaler IC**
- **32MB DDR SDRAM**

**LCD-TV Control IC**

- **Trumtion-Zipro Chip**

**LCD TV Block Diagram**

- **SVC208**
- **SVC230**
- **NTSCPAL**
- **TUNER**
- **LA7585**
- **LA7587/88**
- **LA7565**
- **SVC208**
- **SVC230**
- **LA7585**
- **LA7587/88**
- **LA7565**
- **SWITCH**
- **VIF/SIF**
- **ELECTRONIC VOL**
- **AF/Output**
- **POWERAMP**
- **LC41XX**
- **LC758XX**
- **LCD DRIVER**
- **LCD PANEL**
- **COMPLEX DEVICES (PNP+NPN)**
- **CPH5006**
- **Diodes**
- **DC-DC CONVERTER**
- **DC-AC INVERTER**
- **OSD CONTROLLER**
- **BACK LIGHT**
- **2SC1804T/2SC1802T**
- **2SC5706**
- **PM/2SJ503/2SJ485**
- **CPH3109/3116/3216/3205/3212/5504**
- **FSS140/132/134**
- **CPH3304/3414**
- **SBS004/005/006**
- **LA7221**
- **LA863228**
- **Audio/Video Switch**
- **MICON**
- **LC7458A**
- **LC7454A8A**
- **LA5681**
- **LA683228**
- **NTSCT_AL**
- **VIF/SIF**
- **MICRON**
- **LC7454A8A**
- **LC7454A8A**
- **LA266/4267/4268**
- **LA276/4277/4278**
- **DC-DC CONVERTER**
- **DC-AC INVERTER**
- **OSD CONTROLLER**
- **BACK LIGHT**
- **2SC1804T/2SC1802T**
- **2SC5706**
- **PM/2SJ503/2SJ485**
- **CPH3109/3116/3216/3205/3212/5504**

**De-interlace**

- **example**

- **Best product**
- **Brand recognition**
- **Established market position**

**DCDI™ (Directional Correlational De-Interlacing)** removes objectionable staircase artifacts by using adaptive processing on detected lines and edges.
Luminance of LCD vs. CRT

(a) CRT (Impulse Type)

(b) LCD (Hold Type)

(c) LCD (Impulse-like Type)

Display Quality for Moving Picture: Which is Better?

Black Insertion

- Emulate impulse-type display
  - Turn off backlight
  - Insert black data or clear the data on pixel
  - Double frame rate (60 -> 120 -> 240 Hz)

Adjustable Gamma Curve

Gamma control code (from T-CON)

8-bit Data

Vref [1:18] V0~V255

DAC

Vout

Use external Gamma control code to control final Gamma resistance rings

example

γ−1.8

γ−2.2

γ−2.6
Over 8-bit Color Depth

Over-8 bit data

new DAC

with

$\gamma$-R string

Vref [1:18] $\rightarrow$ Vout (over-8 bit resolution)

8 bit Source driver IC $\rightarrow$ 10 bit $\rightarrow$ 12 bit?

Effect on LC Overdrive

FFD (Feedforward Driving) Method by Mitsubishi

Initial@Gray@Level
Final@Gray@Level

(a) Conventional driving
(b) FFD

Overdrive Circuits

Overdrive

Conventional

Data

Dn+1

Lookups Table

Data'

Memory

address

Read/Write

Control ckt

$T_r + T_i \approx 25$ms (ON/OFF)

$T_r, T_i < 20$ms (Gray Level)
Dynamic Contrast Enhancement

- Over-8 bit color depth
- Dynamic gamma correction
- Dynamic backlight control

Other Technologies

- 10 bit color depth (source driver IC)
  - 1.07 billion colors
- LED backlight
  - R, G, B mixed LED BLU
    - NTSC ratio > 100%
    - R/G/B color sequential method (CF-free)
    - Power consumption
    - Thin module thickness
- Digital Image Processing
  - Sony:WEGA engine...

LCD TV Trends

Technology trends and challenges

<table>
<thead>
<tr>
<th>Size</th>
<th>Challenge</th>
<th>Brightness/C.R.</th>
<th>Response Time</th>
<th>Viewing angle</th>
<th>Resolution</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD Monitor</td>
<td>15-20”</td>
<td>250/400</td>
<td>25~16ms</td>
<td>140/160</td>
<td>XGA~UXGA</td>
</tr>
<tr>
<td>LCD TV</td>
<td>15-20”</td>
<td>400~550</td>
<td>25~16ms</td>
<td>160/160</td>
<td>SVGA~WXGA</td>
</tr>
<tr>
<td></td>
<td>20-30”</td>
<td>&gt;550/&gt;2k</td>
<td>16~12ms</td>
<td>176/176</td>
<td>WUXGA-HDTV</td>
</tr>
<tr>
<td></td>
<td>32-65”</td>
<td>&gt;550/&gt;2k</td>
<td>&lt; 8 ms</td>
<td>160/160</td>
<td></td>
</tr>
</tbody>
</table>

Outline

Ch4. Driving Circuits Design of A-Si TFT

- Gate Driving Circuit
- Source Driving Circuit
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface
Applications of Small Size Display

Mobile phone
- STN
- CSTN
- OLED

DVD Player
- VFD
- STN
- LED

Car Audio
- STN
- OLED

Home Audio
- VFD
- STN
- OLED

Industrial Instrument
- STN
- VFD
- OLED

Small-Size TFT-LCD Driver IC

Controller
- 0.25 μm

Source driver
- 0.5 μm

DC/DC converter
- 0.6 μm HV

Gate driver
- 0.6 μm HV

Controller + Source driver

DC/DC converter + gate driver

Single chip HV

Small-Size TFT-LCD Driver IC

4 Chip
- TCP/COF Type

2 Chip
- COG/COF Type

1 Chip
- COG Type

Architectures of One Chip TFT-LCD Driver IC

Simple IC Sketch for TFT Mobile Phone
- 2.5V Block: OSC, SRAM, APR, Some Logic
- 5V Block: I/O, Source, Regulator, Charge Pump (PWR)
- 32/40V Block: Gate, Regulator, Charge Pump (PWR)

Architecture of One Chip TFT-LCD Driver IC

Single Chip TFT-LCD Driver IC for Mobile Phone Application

Gate Driver
- PWR

Source Driver
- SRAM
- GAMA64
- APR
- SRAM

Gate Driver
- PWR

System Interface
- 18/16/9-bit parallel, 3-pin SPI

Gate control

Gamma adjusting
graylevel generator

Power supply circuit

Address
counter

Index register

Control register

Timing
generator

Gate driver

VGH
VGL
Vcom
OSC

VDD
VDD3

396 Channel
driver

Soft
drive

Built-in GRAM
132x18x176 bit

Read/Write
Data latch

System Interface
18/16/9-bit parallel, 3-pin SPI
Voltage Setting

VGH(+9 ~ +16.5V)
AVDD(+3.5~ +5.5V)
VCOM(VCL+0.5 to 1.0V)
VcomL(VCL+0.5 to 1.0V)
GND(0V)

Note:
adjust the conditions of AVDD-GVDD > 0.5V, VcomL-VCL > 0.5V, and VgoffL-VGL > 0.5V with loads becauseThey differ depending on the display load to be driven. In addition, Vci can be directly input to Vci1.

Power Pins Description (1/2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>-</td>
<td>System power supply. As NT3911 has internal regulator, VDD range varies with each mode. Non-regulated mode (PregB = 1): +2.0 ~ +2.5 V Regulated mode (PregB = 0): +2.0+ V</td>
</tr>
<tr>
<td>VDD3</td>
<td>-</td>
<td>System power supply for regulator as external power. (VDD3: +2.5 ~ +3.5 V)</td>
</tr>
<tr>
<td>AVDD</td>
<td>I/O</td>
<td>A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: +3.0 ~ +5.5 V)</td>
</tr>
<tr>
<td>GVDD</td>
<td>I/O</td>
<td>Standard level for grayscale voltage generator. Connect a capacitor for stabilization.</td>
</tr>
<tr>
<td>VCI</td>
<td>I/O</td>
<td>An internal reference power supply for VREG1OUT/VREG2OUT. Connect this pin to VCI2 pin. When using a charge-pump circuit 1, leave it open.</td>
</tr>
<tr>
<td>VSS</td>
<td>I/O</td>
<td>System ground (0V)</td>
</tr>
<tr>
<td>AVSS</td>
<td>-</td>
<td>System ground for analog circuit block.</td>
</tr>
<tr>
<td>VCL</td>
<td>I/O</td>
<td>A power supply pin for generating VcomH. When VcomH is higher than VSS, outputs VSS level.</td>
</tr>
<tr>
<td>REGP</td>
<td>I/O</td>
<td>Input pins for reference voltages of VREG1OUT when the internal reference-voltage generation circuit is not used. Leave these pins open when the internal reference-voltage generation circuit is used.</td>
</tr>
<tr>
<td>VREG1OUT</td>
<td>0</td>
<td>This pin outputs a reference voltage for VREG1 between AVDD and VSS. When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGG. Connect this pin to a capacitor for stabilization. When this pin is not used, leave it open.</td>
</tr>
<tr>
<td>VREG2OUT</td>
<td>0</td>
<td>This pin outputs a reference voltage for VREG2 between VSS and VCL. When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGG. Connect this pin to a capacitor for stabilization. When this pin is not used, leave it open.</td>
</tr>
<tr>
<td>VcomOUT</td>
<td>0</td>
<td>A power supply for the TFT display counter electrode. The alternating cycle can be set by the M pin. Connect this pin to the TFT display counter electrode.</td>
</tr>
</tbody>
</table>

Voltage Waveforms

VGH(+9 ~ +16.5V)
AVDD(+3.5~ +5.5V)
VcomH(+3.0~ VREG1OUT)
VcomL(VCL+0.5 to 1.0V)
VcomH(VCL+0.5 to 1.0V)
VcomL(VCL+0.5 to 1.0V)
VcomH(VCL+0.5 to 1.0V)
VcomL(VCL+0.5 to 1.0V)

Power Pins Description (2/2)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>VcomR</td>
<td>I</td>
<td>A reference voltage of VcomH. When VcomH is externally adjusted, half the internal adjuster of VcomH by setting the register and insert a variable resistor between VREG1OUT and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.</td>
</tr>
<tr>
<td>VcomH</td>
<td>O</td>
<td>This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.</td>
</tr>
<tr>
<td>VcomL</td>
<td>O</td>
<td>When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization.</td>
</tr>
<tr>
<td>VGH</td>
<td>O</td>
<td>A negative power output pin for gate driver, internal charge-pump circuits, bias circuits, and operational amplifiers. Connect this pin to VDV4 pin. When not using a charge-pump circuit 2, leave it open.</td>
</tr>
<tr>
<td>VGL</td>
<td>O</td>
<td>A power output pin for gate driver. This pin is a negative voltage for the gate off level. Connect this pin to VgoffOUT. When VgoffOUT is not used, connect an external-voltage power supply higher than -15.0 V.</td>
</tr>
<tr>
<td>VcGoff</td>
<td>I</td>
<td>Power supply pin for off level for gate of TFT. Connect this pin to VgoffOUT. When VgoffOUT is not used, connect an external-voltage power supply higher than -7.8 V.</td>
</tr>
<tr>
<td>VgoffL</td>
<td>O</td>
<td>An power output pin for gate driver. Connect this pin to VcGoff. When VgoffOUT is not used, connect an external-voltage power supply higher than -15.0 V.</td>
</tr>
<tr>
<td>VgoffH</td>
<td>O</td>
<td>Connect this pin to VcGoff. When VgoffOUT is not used, connect an external-voltage power supply higher than -7.8 V.</td>
</tr>
<tr>
<td>VcomL</td>
<td>O</td>
<td>Connect this pin to a capacitor for stabilization. When the internal reference-voltage generation circuit is used, this pin outputs a voltage between VcomH and VcomL. Connect this pin to a capacitor for stabilization.</td>
</tr>
<tr>
<td>VcomH</td>
<td>O</td>
<td>Connect this pin to a capacitor for stabilization. When the internal reference-voltage generation circuit is used, this pin outputs a voltage between VcomH and VcomL. Connect this pin to a capacitor for stabilization.</td>
</tr>
<tr>
<td>VcomL</td>
<td>O</td>
<td>Connect this pin to a capacitor for stabilization. When the internal reference-voltage generation circuit is used, this pin outputs a voltage between VcomH and VcomL. Connect this pin to a capacitor for stabilization.</td>
</tr>
</tbody>
</table>

Note:
VcomR: A reference voltage of VcomH. When VcomH is externally adjusted, half the internal adjuster of VcomH by setting the register and insert a variable resistor between VREG1OUT and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
Power Definition (1/2)

(For the analog circuit)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Nom.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>LCD Supply Voltage</td>
<td>AVDD</td>
<td>3.5</td>
<td>-</td>
<td>5.5</td>
<td>V</td>
<td>For the analog circuit</td>
</tr>
<tr>
<td></td>
<td>VGH</td>
<td>9</td>
<td>-</td>
<td>16.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VOL</td>
<td>-16.5</td>
<td>-</td>
<td>-2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VDDFF</td>
<td>-16</td>
<td>-</td>
<td>-4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>GVDD</td>
<td>3</td>
<td>-</td>
<td>5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Internal reference voltage power supply voltage</td>
<td>VCI</td>
<td>2.5</td>
<td>-</td>
<td>3.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltage deviation</td>
<td>Vod</td>
<td>-</td>
<td>±20</td>
<td>-</td>
<td>mV</td>
<td>Source Driver</td>
</tr>
<tr>
<td>Output Offset between Chips</td>
<td>Vos</td>
<td>-</td>
<td>±20</td>
<td>-</td>
<td>mV</td>
<td>Source Driver</td>
</tr>
<tr>
<td>Dynamic Range of Output</td>
<td>Vdr</td>
<td>0.1</td>
<td>-</td>
<td>GVDD-0.1</td>
<td>V</td>
<td>S1＝3.96</td>
</tr>
<tr>
<td>Source Driver Driving Current of Outputs</td>
<td>ISOH</td>
<td>50</td>
<td>-</td>
<td>-</td>
<td>μA</td>
<td>$S_1$ ＝ 3.96V, $V_{DD}=4.5V ± 3.5V,$ $AVDD=5V$, Gradation output</td>
</tr>
<tr>
<td>Gate Driver Sinking Current of Outputs</td>
<td>IGOL</td>
<td>1</td>
<td>-</td>
<td>-</td>
<td>μA</td>
<td>$G_0 ＝ G_{17}$, $V_{DD}=12V ± 11.5V,$ $V_{GH}=5V$, $V_{GH}=20V$</td>
</tr>
<tr>
<td>Gate Driver Driving Current of Outputs</td>
<td>ISOH</td>
<td>250</td>
<td>-</td>
<td>-</td>
<td>μA</td>
<td>$G_0 ＝ G_{17}$, $V_{DD}=12V ± 17.5V,$ $V_{GH}=5V$, $V_{GH}=20V$</td>
</tr>
<tr>
<td>Power Consumption for Stand-by mode</td>
<td>Isc</td>
<td>-</td>
<td>-</td>
<td>5</td>
<td>μA</td>
<td>No load, $VDD=3V$, $VDD=2V$, $VCI=2.7V$, $VCH=0V$, and all operating is stopped</td>
</tr>
<tr>
<td>Operating Current</td>
<td>IVDD</td>
<td>-</td>
<td>200</td>
<td>500</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>IVCI</td>
<td>-</td>
<td>1.5</td>
<td>2.0</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>

(VDD≤2.0V, VDD3≥3V, VSS≤0V, TA=25℃)

Power Definition (2/2)

(For the regulator circuit)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference voltage for internal digital power</td>
<td>RVDD</td>
<td>1.95</td>
<td>2.0</td>
<td>2.1</td>
<td>V</td>
<td>$VDD=3.3V$</td>
</tr>
<tr>
<td>RVDD driving current</td>
<td>IVVDD</td>
<td>-</td>
<td>200</td>
<td>500</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>Reference voltage for VREG1/OUT</td>
<td>VREG1</td>
<td>5.71</td>
<td>5.83</td>
<td>5.95</td>
<td>V</td>
<td>$VDD=3.3V$, $V_{REG2}=200V$, $VRL3=0V$</td>
</tr>
<tr>
<td>VREG1/OUT driving current</td>
<td>IREG1</td>
<td>1</td>
<td>-</td>
<td>2.5</td>
<td>mA</td>
<td>$VDD=3.3V$, $V_{REG2}=200V$, $VRL3=0V$</td>
</tr>
<tr>
<td>Reference voltage for grayscale voltage generator</td>
<td>VREG2</td>
<td>0.47</td>
<td>-6.6</td>
<td>-6.73</td>
<td>V</td>
<td>$VDD=3.3V$, $VRL3=0V$</td>
</tr>
<tr>
<td>VREG2/OUT driving current</td>
<td>IREG2</td>
<td>-500</td>
<td>-</td>
<td>-100</td>
<td>μA</td>
<td>$VDD=3.3V$, $VRL3=0V$</td>
</tr>
<tr>
<td>GVDD driving current</td>
<td>IVVDD</td>
<td>100</td>
<td>-</td>
<td>150</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>High level reference voltage of Vgoff</td>
<td>VgoffH</td>
<td>-0.85</td>
<td>-0.83</td>
<td>-0.81</td>
<td>V</td>
<td>$VDD=3.3V$, $V_{REG2}=200V$, $VRL3=0V$, $VDD=4V$</td>
</tr>
<tr>
<td>Low level reference voltage of Vgoff</td>
<td>VgoffL</td>
<td>-0.47</td>
<td>-0.66</td>
<td>-0.73</td>
<td>V</td>
<td>$VDD=3.3V$, $VRL3=0V$</td>
</tr>
<tr>
<td>High level reference voltage of Vcom</td>
<td>VCOMH</td>
<td>4.57</td>
<td>4.66</td>
<td>4.75</td>
<td>V</td>
<td>$VDD=3.3V$, $V_{REG2}=200V$, $VRL3=0V$, $VDD=4V$</td>
</tr>
<tr>
<td>Low level reference voltage of Vcom</td>
<td>VCOML</td>
<td>-1.13</td>
<td>-1.11</td>
<td>-1.09</td>
<td>V</td>
<td>$VDD=3.3V$, $V_{REG2}=200V$, $VRL3=0V$, $VDD=4V$</td>
</tr>
</tbody>
</table>

(Gamma ADJUSTMENT FUNCTION)

- The NT3911 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels.

Configuration of the Internal Power-supply Circuit

GAMMA ADJUSTMENT FUNCTION
Scan Mode

- Gate scan mode of NT3911 is set by SM and GS bit. GS bit determines the scan direction whether the gate driver scans forward or reverse direction. SM bit determines the method of display division (Even/Odd or Upper/Lower division drive). Using this function, various connections between NT3911 and the liquid crystal panels can be accomplished.

<table>
<thead>
<tr>
<th>SM</th>
<th>GS</th>
<th>Scan Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>A</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>B</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>C</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>D</td>
</tr>
</tbody>
</table>

Structure of Grayscale Amplifier

- The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Each level is split by the internal ladder resistance and level between V0 to V63 is generated.

Gamma Adjustment Register

- This block has the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4-type of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (average <R><G><B> are common.) The following figure indicates the operation of each adjusting register.

Chip Size & Pad Dimensions

- NOTES:
  - Scribe line included in this chip size (Scribe line: 120um)
Process Feature for One Chip Driver IC

<table>
<thead>
<tr>
<th>Technology</th>
<th>0.25um</th>
</tr>
</thead>
<tbody>
<tr>
<td>LV (Dual Gate) / HV</td>
<td>2.5V / 5V / 40V (+/-20V)</td>
</tr>
<tr>
<td>Oxide Thickness</td>
<td>48A / 110A / 1000A</td>
</tr>
<tr>
<td>40V HVMOS Structure</td>
<td>LDMOS</td>
</tr>
<tr>
<td>LV / HV Well Structure</td>
<td>Retrograde / Drive-In Well + NBL</td>
</tr>
<tr>
<td>Isolation</td>
<td>STI / P-EPI</td>
</tr>
<tr>
<td>Gate Material</td>
<td>Poly (S/D Implant Doped) + Salicide</td>
</tr>
<tr>
<td>S / D Area</td>
<td>Salicide</td>
</tr>
<tr>
<td>Capacitor</td>
<td>MIM</td>
</tr>
<tr>
<td>High Rs Poly</td>
<td>400~2000 Ohm</td>
</tr>
</tbody>
</table>

Source: Novatek training material

Product Applications

- TFT Driver IC for Mobile Phone
  - Amorphous-Silicon TFT Mobile Phone Driver IC Product Line
    
    | Panel Category | NT3911 | NT3912 | NT391X | NT391X |
    |----------------|--------|--------|--------|--------|
    | Display Size   | 132x176| 176x240| X      | X      |
    | Display Color  | 262k   | 262k   | 262k   | 262k   |
    | SRAM Size      | 418k   | 760k   | X      | X      |

- STN Driver IC for Mobile Phone
  - NT7523为Hi-Fas CSTN One Chip Driver IC，使用0.25μm 2.5/5/32V Process

Source: Novatek training material

LV and HV Device Type

- LV and HV Device Type and Related Data (1)
- 2.5 / 5V Devices Characterization
  - 5 LV Devices (2.5V NMOS and PMOS, 5V NMOS and PMOS, 2.5V Native NMOS)
  - STI Field Isolation
  - Triple Well Structure
  - Salicide Structure
- 2.5 / 5V Devices Cross Section Sketch

LTPS TFT-LCD Driver ICs

- Conventional a-Si TFT-LCD
- LTPS TFT-LCD Example 1
- LTPS TFT-LCD Example 2

Source: Novatek training material
Outline

Ch4. Driving Circuits Design of A-Si TFT
- Gate Driving Circuit
- Source Driving Circuit
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface

Interfaces in TFT-LCD Monitor

Digital vs. Analog

<table>
<thead>
<tr>
<th></th>
<th>TMDS</th>
<th>Analog RGB</th>
</tr>
</thead>
<tbody>
<tr>
<td>signal</td>
<td>Digital</td>
<td>Analog</td>
</tr>
<tr>
<td>Tx distance</td>
<td>&gt;5M</td>
<td>&lt;2M</td>
</tr>
<tr>
<td>Image quality</td>
<td>Good</td>
<td>Bad</td>
</tr>
<tr>
<td></td>
<td>Differential pair</td>
<td>Depend on cable and noise</td>
</tr>
<tr>
<td></td>
<td>Low swing</td>
<td>Depend on ADC</td>
</tr>
<tr>
<td>other</td>
<td>TMDS Tx in Graphic card is needed</td>
<td>DAC in Graphic card is needed</td>
</tr>
<tr>
<td></td>
<td>TMDS Rx in scaler is needed</td>
<td>ADC in scaler is needed</td>
</tr>
</tbody>
</table>

Panel Input Interface

<table>
<thead>
<tr>
<th></th>
<th>resolution</th>
<th>Interface</th>
<th>1/2 port</th>
<th>Freq.</th>
</tr>
</thead>
<tbody>
<tr>
<td>NB</td>
<td>XGA</td>
<td>LVDS</td>
<td>1</td>
<td>65MHZ</td>
</tr>
<tr>
<td></td>
<td>SXGA, SXGA+</td>
<td>LVDS</td>
<td>2</td>
<td>54MHZ</td>
</tr>
<tr>
<td>Monitor</td>
<td>XGA</td>
<td>TTL</td>
<td>2</td>
<td>32.5MHZ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>LVDS</td>
<td>1</td>
<td>65MHZ</td>
</tr>
<tr>
<td></td>
<td>SXGA, SXGA+</td>
<td>LVDS</td>
<td>2</td>
<td>54MHZ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TTL</td>
<td>2</td>
<td>54MHZ</td>
</tr>
<tr>
<td></td>
<td>UXGA</td>
<td>LVDS</td>
<td>2</td>
<td>81MHZ</td>
</tr>
</tbody>
</table>
### TTL vs. LVDS

<table>
<thead>
<tr>
<th></th>
<th>TTL</th>
<th>LVDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin count</td>
<td>60~80pin Connector + large PCB area and data bus</td>
<td>50~30pin Connector + small PCB area and data bus</td>
</tr>
<tr>
<td>Cost</td>
<td>cheap</td>
<td>expensive(Tx/Rx)</td>
</tr>
<tr>
<td></td>
<td>PCB large</td>
<td>PCB small</td>
</tr>
<tr>
<td></td>
<td>Extra R.C. bead in input data</td>
<td>Extra R.C. bead in input data is not needed</td>
</tr>
<tr>
<td>Signal quality</td>
<td>Bad ➔ Data coupling</td>
<td>Good ➔ differential pair</td>
</tr>
<tr>
<td>Distance</td>
<td>Short</td>
<td>Longer</td>
</tr>
<tr>
<td>Frequency</td>
<td>Operation in low frequency</td>
<td>Can operation in high frequency</td>
</tr>
<tr>
<td>EMI</td>
<td>Bad +3.3V</td>
<td>Good + Vcom=1.2V swing=350mV</td>
</tr>
<tr>
<td></td>
<td>Extra R.C. bead is needed for reducing EMI</td>
<td>+ terminal resistor is needed</td>
</tr>
<tr>
<td>Power consumption (bus)</td>
<td>High(3.3V)</td>
<td>low</td>
</tr>
<tr>
<td>Application</td>
<td>Monitor</td>
<td>NB/Monitor</td>
</tr>
</tbody>
</table>

### Comparison of TTL, RSDS, and Mini-LVDS

<table>
<thead>
<tr>
<th></th>
<th>TTL</th>
<th>RSDS</th>
<th>Mini-LVDS</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bus lines</td>
<td>8-bit</td>
<td>24X2</td>
<td>24</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>6-bit</td>
<td>18X2</td>
<td>18</td>
<td>10</td>
</tr>
<tr>
<td>Voltage Swing</td>
<td>3.3V</td>
<td>200mV</td>
<td>200mV</td>
<td>Lower amplitude for reducing EMI</td>
</tr>
<tr>
<td>Frequency</td>
<td>XGA</td>
<td>32.5M (2 ports)</td>
<td>67M (1 port)</td>
<td>67M (2 ports)</td>
</tr>
<tr>
<td></td>
<td>SXGA</td>
<td>54M (2 ports)</td>
<td>54M (2 ports)</td>
<td>108M (2 ports)</td>
</tr>
<tr>
<td></td>
<td>UXGA</td>
<td>-</td>
<td>81M</td>
<td>162M</td>
</tr>
<tr>
<td>LCD Application</td>
<td></td>
<td>~SXGA</td>
<td>~UXGA</td>
<td>~QXGA</td>
</tr>
<tr>
<td>PCB Area</td>
<td>1</td>
<td>0.7~0.8</td>
<td>0.5~0.7</td>
<td><del>0.5</del>0.7</td>
</tr>
<tr>
<td>T-CON Pins</td>
<td>6-bit</td>
<td>~100</td>
<td>~64</td>
<td>~100</td>
</tr>
<tr>
<td>Driver IC Input Pins</td>
<td>6-bit</td>
<td>~90</td>
<td>~60</td>
<td>~50</td>
</tr>
</tbody>
</table>

Remark: RSDS and Mini-LVDS use twin-pair lines

### RSDS Definition

- **Reduced Swing Differential Signal**
  - ±200 mV swing (typical)
  - 2:1 mux - 2 data per clock cycle
  - 100 ohm differential terminals
  - Voffset = 1.2 V
  - RGB data and clock only
- **Apply to bus between T-Con and source drivers**
  - Reduce EMI
  - Reduce power consumption
  - Reduce source driver bus width

### 8 Bit RGB RSDS Data

- **Start pulse**
- **Invalid data**
- **Current Flow out of page**
- **Current Flow in to page**
RSDS Features and Benefits

- **Reduced pin T-Con counts**
  - Enable smaller area PCBs

- **Reduced number of components**
  - Small area PCBs
  - Lower cost
  - Number of components: TTL:RSDS = 190:101 (in 14.1" XGA) → 46.8% reduction

- **Reduced number of PCB layers**
  - Number of layers: TTL:RSDS = 6:4

**Mini-LVDS**

- 6 bit data, 5 pairs
**Point to Point Differential Signaling (PPDS)**

- PPDS is based largely on the RSDS™
- Advantages:
  - The total number of input signals for each column driver is greatly reduced.
    - 8-bit RSDS system: 12 data pairs and the clock pair by each column driver.
    - In a PPDS system: signal data pair and a clock pair
    - 26 in RSDS → 4 in PPDS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>RSDS</th>
<th>PPDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Signal Level</td>
<td>±200mV</td>
<td>±200mV</td>
</tr>
<tr>
<td>Common Mode Voltage</td>
<td>1.3V</td>
<td>0.8V</td>
</tr>
<tr>
<td>Typical Output Current</td>
<td>2mA</td>
<td>2mA</td>
</tr>
<tr>
<td>Transmission Lines</td>
<td>50Ω</td>
<td>50Ω</td>
</tr>
</tbody>
</table>

Table 1. Comparison of PPDS and RSDS levels

**RSDS vs. Mini-LVDS**

- **RSDS is the major interface**
- **Mini-LVDS become important for high resolution panel**

<table>
<thead>
<tr>
<th></th>
<th>RSDS</th>
<th>Mini-LVDS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCB Size</td>
<td>Larger</td>
<td>Smaller</td>
</tr>
<tr>
<td>TCON</td>
<td>XGA: TQFP64/80</td>
<td>SXGA/UXGA: TQFP128/144</td>
</tr>
<tr>
<td>Driver Size</td>
<td>Same</td>
<td>Same</td>
</tr>
<tr>
<td>Frequency Limitation</td>
<td>DIO(Start Pulse)</td>
<td>No</td>
</tr>
<tr>
<td>Resolution Limitation</td>
<td>&lt;= UXGA/Dual Buses</td>
<td>QXGA or larger/Dual Buses</td>
</tr>
<tr>
<td>Possible Driver Vendors</td>
<td>More</td>
<td>Limited</td>
</tr>
</tbody>
</table>

**PPDS™**

- Advantages: (cont.)
  - improved signal integrity.
    - typical RSDS bus architecture
    - vias and stubs on every signal line creates a large number of impedance discontinuities.
    - point to point system no vias and stubs data signal maintain higher level Higher color depth
  - Major improvement in EMI
    - Due to the incoming LVDS clock and PPDS clock operating at different frequency.
PPDS Protocol

- The total reduction in data signals from an RSDS based system to the PPDS architecture.
- The protocol is split into 5 required interval and 1 optional interval.

Figure 3. Total number of traces for the PPDS interface compared to RSDS

Summaries

Technology Trends of Large-Size TFT-LCD Source Driver IC

<table>
<thead>
<tr>
<th>Resolution</th>
<th>XGA</th>
<th>SXGA</th>
<th>UXGA</th>
<th>WUXGA/HDTV</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1024x768)</td>
<td>(1280x1024)</td>
<td>(1600x1200)</td>
<td>(1920x1200)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Color Depth</th>
<th>6-bit</th>
<th>8-bit</th>
<th>10-bit</th>
</tr>
</thead>
<tbody>
<tr>
<td>(64灰階)</td>
<td>(256灰階)</td>
<td>(1024灰階)</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Type</th>
<th>TN+Film</th>
<th>MVA/IPS</th>
<th>OCB</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R60/L60/U60/D40)</td>
<td>(R80/L80/U80/D80)</td>
<td>8~10V</td>
<td></td>
</tr>
<tr>
<td>Pitch 50~70um</td>
<td>Pitch 30~50um</td>
<td>12~17V</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Pin Count</th>
<th>300~384 pin</th>
<th>384/480 pin</th>
<th>480 pin</th>
<th>&gt;500 pin</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pitch 50~70um</td>
<td>Pitch 30~50um</td>
<td>Overdrive</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Technology</th>
<th>TCP</th>
<th>COG</th>
<th>COF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data Speed</td>
<td>50~70 MHz</td>
<td>60~85 MHz</td>
<td></td>
</tr>
</tbody>
</table>