Flat Panel Display : Principle and Driving Circuit Design

Chapter 4

Driving Circuit Design of A-Si TFT

中興大學電機系 / 汪芳興

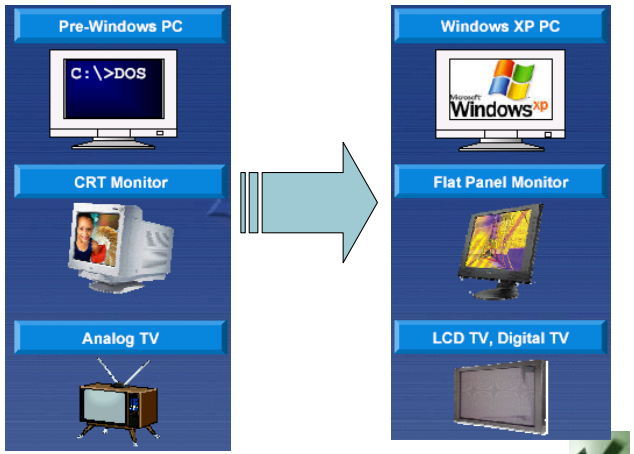
Outline

Ch4. Driving Circuits Design of A-Si TFT

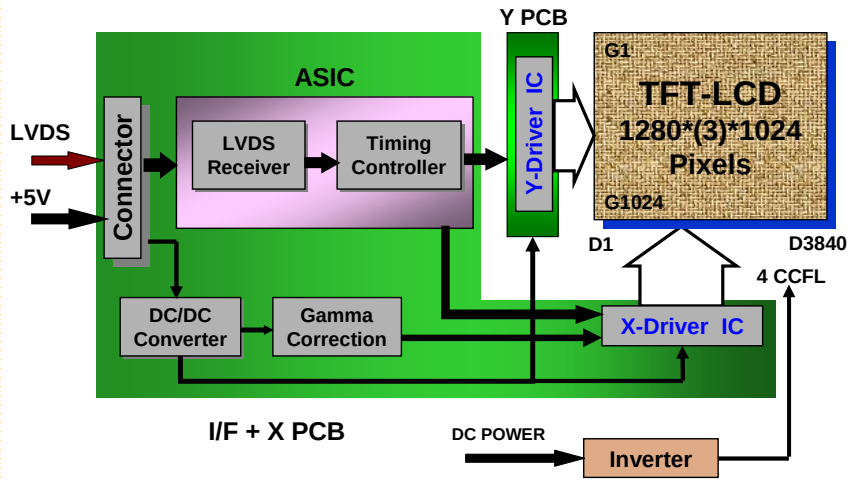
- Gate Driving Circuit
- Source Driving Circuit
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface

Introduction to LCD Driver IC

- **Improved Visualization:**
  - A Fundamental Market Enabler

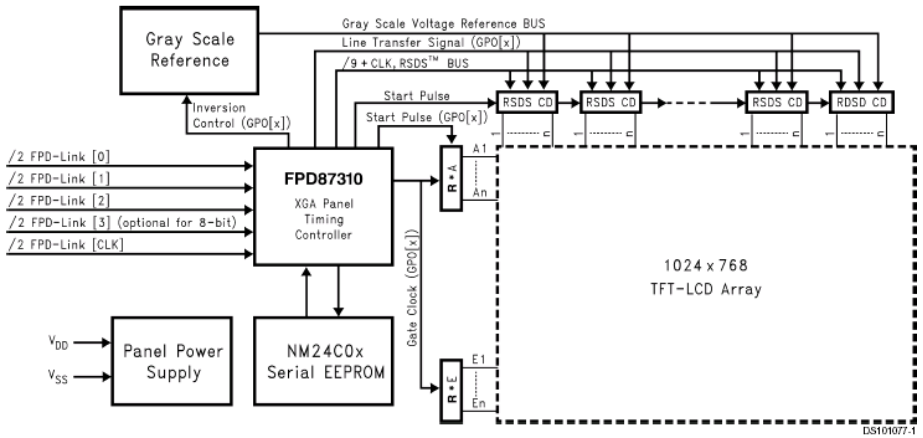


Driving Circuits of TFT- LCD Module



Driving Circuits of TFT- LCD Module

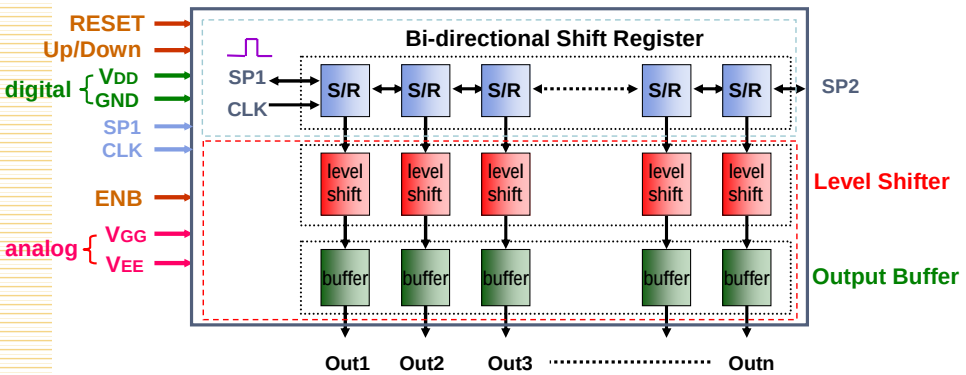
- Example



Gate Driver IC

- Also called scan driver or row driver
- Function
  - Read in start signal
  - Progressively turn on pixel TFTs on each gate line
  - Turn off TFT during pixel holding period
- Design consideration
  - RC delay of bus line (for large-size panel)
- Capacitive coupling driving (CC driving)
- Gate-driver in panel

Gate Driver Architecture

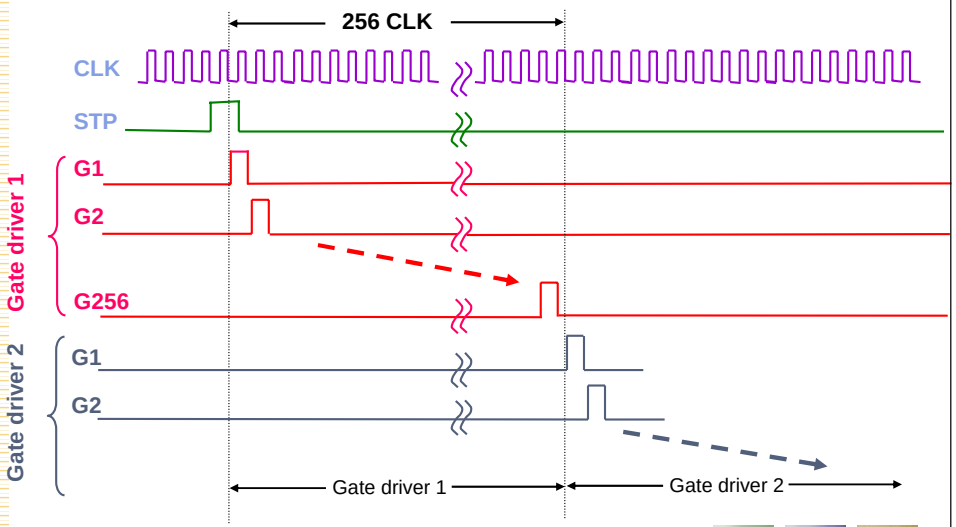


To Display Area

S/R frequency : 10k~75kHz , Output voltage range : > 12V

Gate driver IC 電路方塊圖

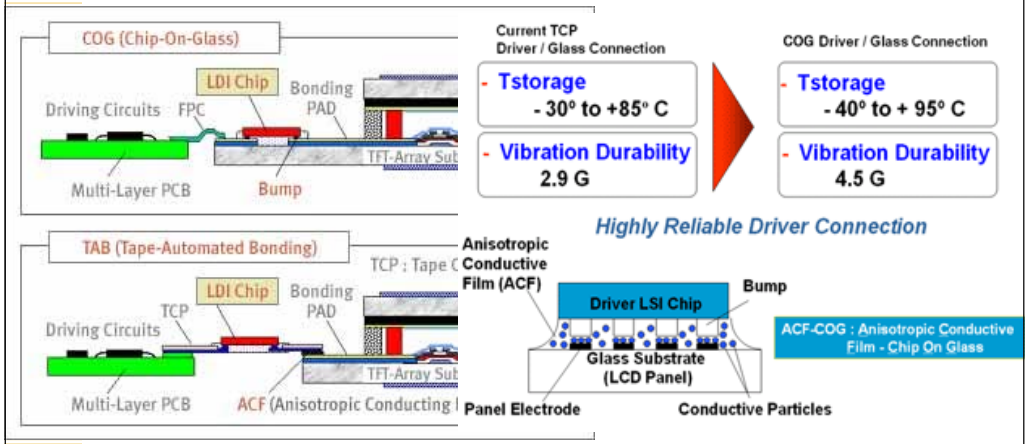
Timing of Gate Driver



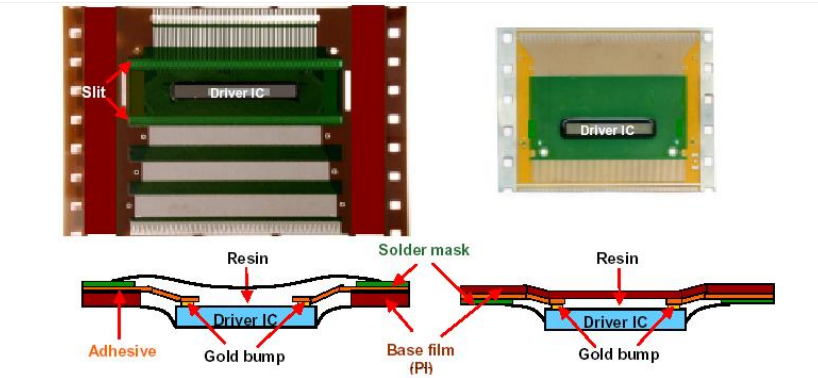
Key Specifications

- Channel number (240,256,264,270,300,308…)
- Max. operation frequency (200KHz, 500KHz)
- 2 level or 3 level driving
- Operation voltage
  - digital : 5V, 3.3V
  - analog : V_{GG}>20V, V_{EE}<-10V
- Package (TCP, COG, COF)

Package of Driver IC

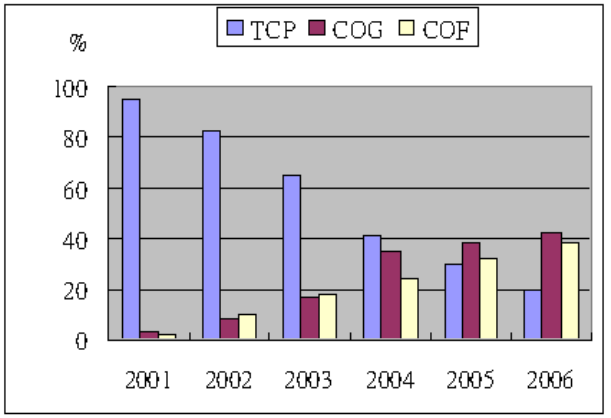


Package of Driver IC



Package of Driver IC

圖一 大型面板驅動 IC 需求比例結構



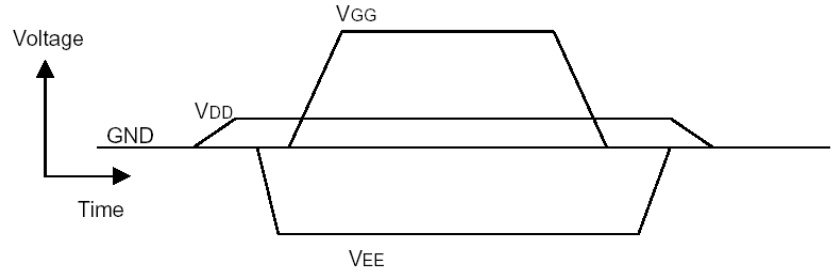
Source: 拓墣產業研究所整理 2005/10

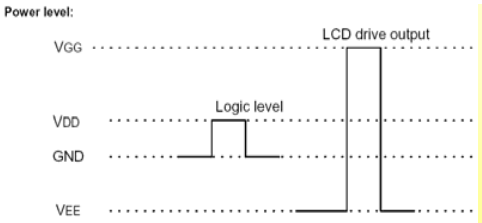
Channel Number vs. Resolution

- Gate driver : No. of driver and No. of output channel

	lines	6	5	4	3
VGA	480			120	
SVGA	600		120	150	200
XGA	768	128	154	192	256
SXGA	1024			256	
UXGA	1200		240	300	

Power On/Off Sequence

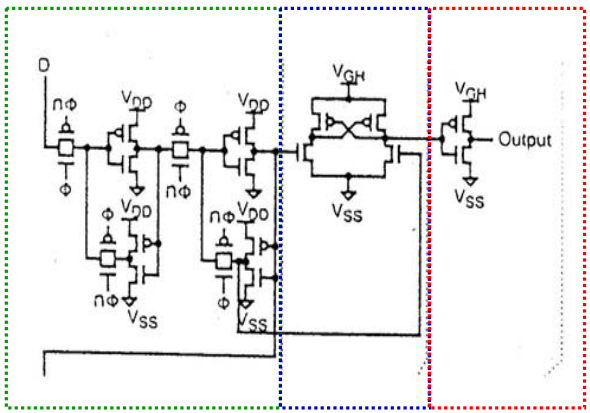




This IC is a high-voltage LCD driver, so it may be damaged by a large current flow if an incorrect power sequence is used. Connecting the drive powers, VEE & VGG, after the logical power, VDD, is the recommended sequence.

Gate Driver Circuits

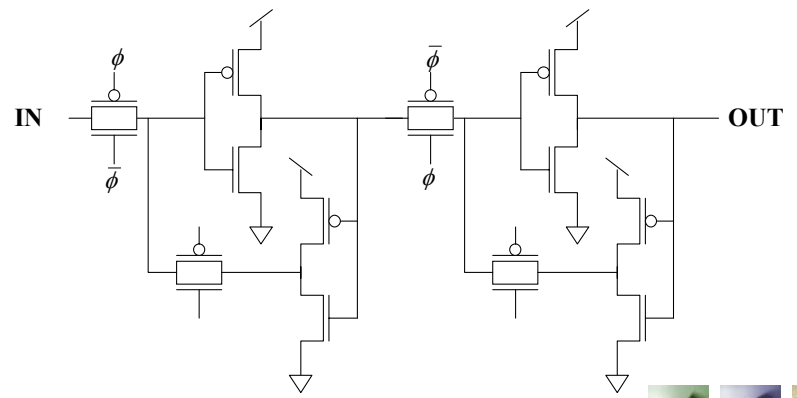
Example



Shift register **Level shifter** **Buffer**

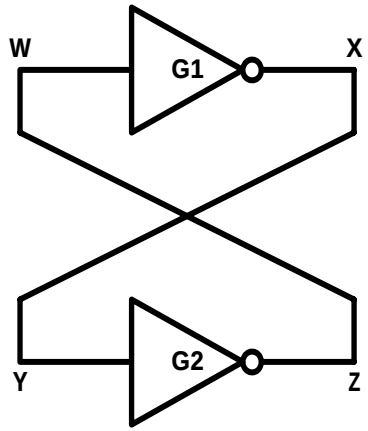
CMOS Shift Register

Static S/R

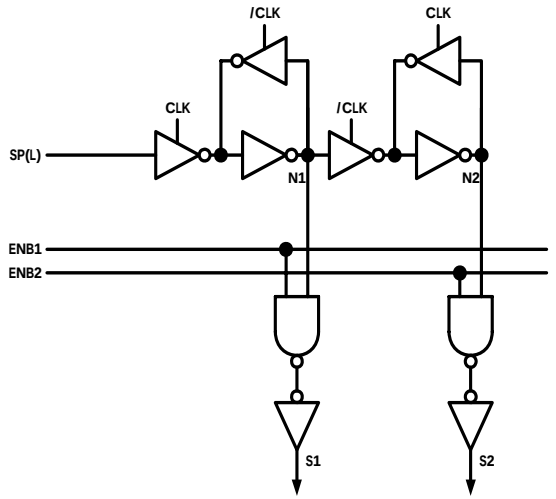


Shift Register

- Latch
  - Basic memory element
  - Two cross-coupled logic inverter
  - Bistable circuit

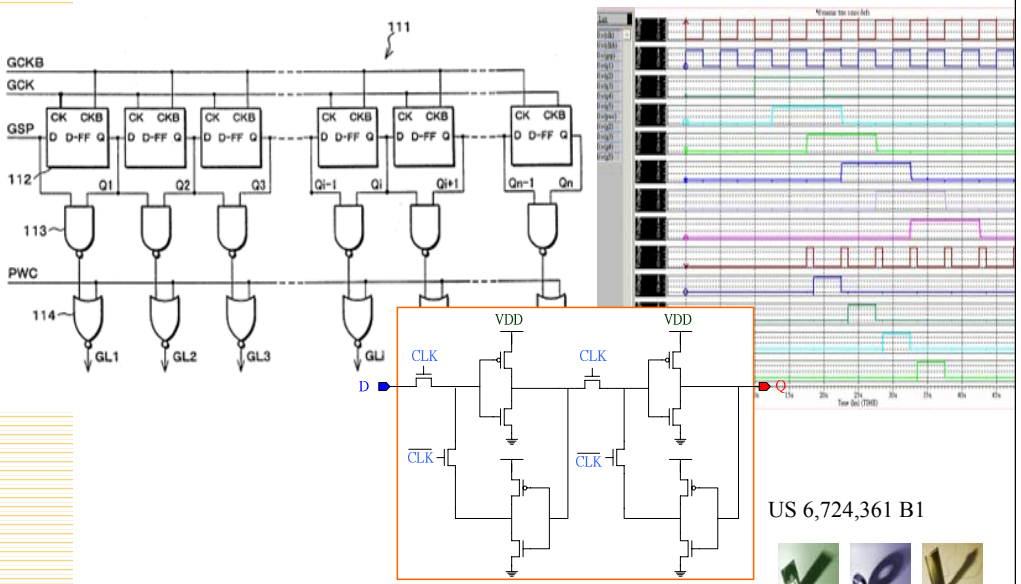


Shift Register – Latch 1



US 6,157,361
SHARP

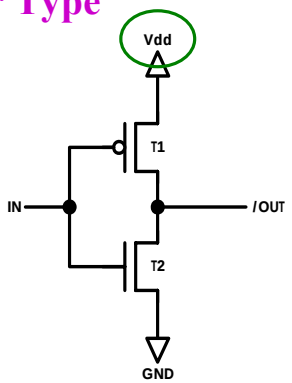
Shift Register – Latch 2

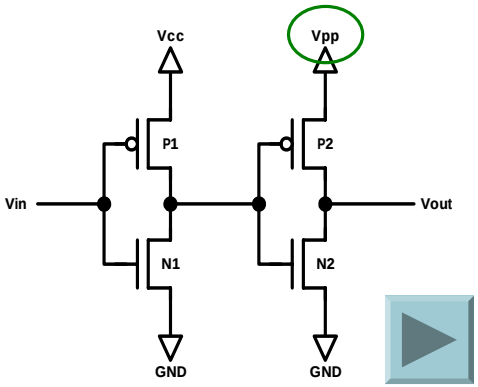


US 6,724,361 B1

Level Shifter – Example 1

Inverter Type

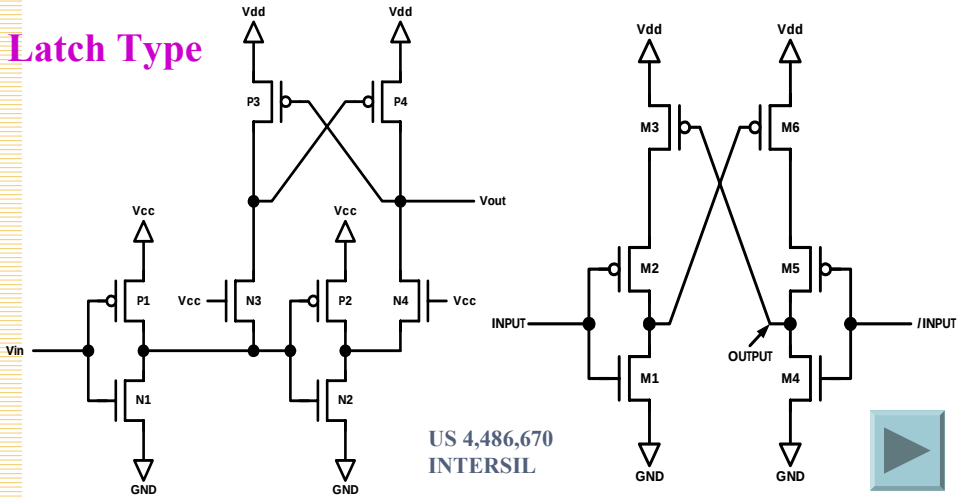




➢ With both transistors of the inverters turned on, a current path from the supply voltage to ground is present, resulting in **undesirable power consumption.**

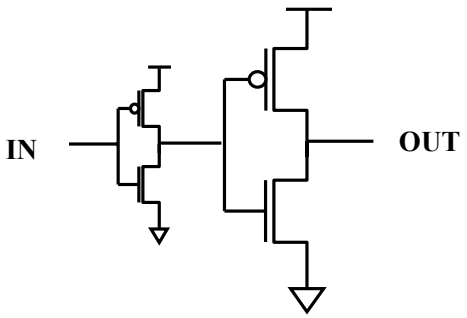
Ref : Low Power Digital VLSI Design, A. Bellaouar, M. Elmasry

Level Shifter – Example 2



➢ This circuit overcomes the problem of direct power consumption by using a latch.

Output Buffer



Area ratio = *e* (2.7) ~ 3

TSMC HV Process

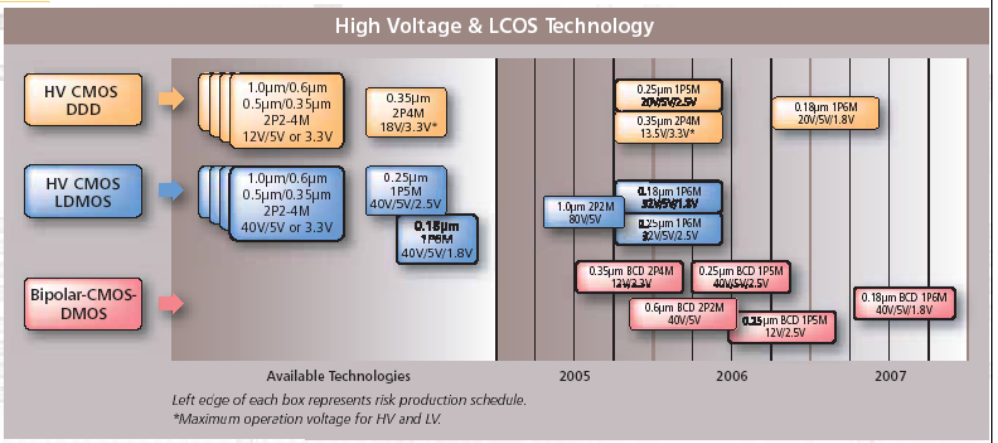
High Voltage Process Characteristics

Technology	0.35-micron			0.25-micron	0.18-micron
	1-2P4M			1P5M	1P6M
HV / LV	12V / 3.3V	18V / 3.3V	40V / 3.3V	40V / 5V / 2.5V	40V / 5V / 1.8V
HV device structure	DDD	DDD	LDMOS	LDMOS	LDMOS
Well	Twin Well	Twin Well	Quad Well	Quad Well	Quad Well
Isolation	LOCOS			STI	
Capacitor type	PiP			MiM	
Idsat_N/P_HV (nA/μm)	400 / 250	260 / 170	400 / 230	400 / 230	400 / 230
Major Application	LCD Source Driver		LCD Gate Drive Power IC	One Chip Small Panel LCD Driver	
Process Ready	Yes	Yes	Yes	Yes	Yes
Logic Compatible	Yes				

Source : Web of TSMC

Roadmap of High Voltage Technology

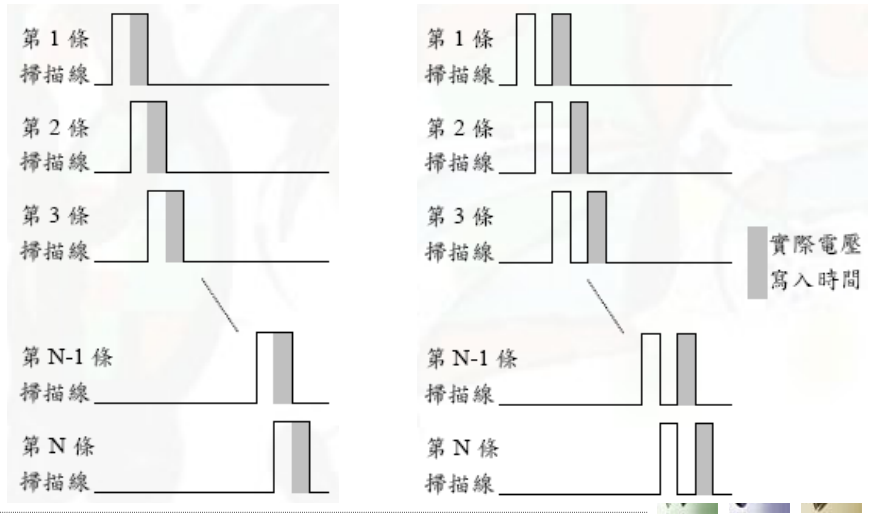
- Roadmap of TSMC HV technology



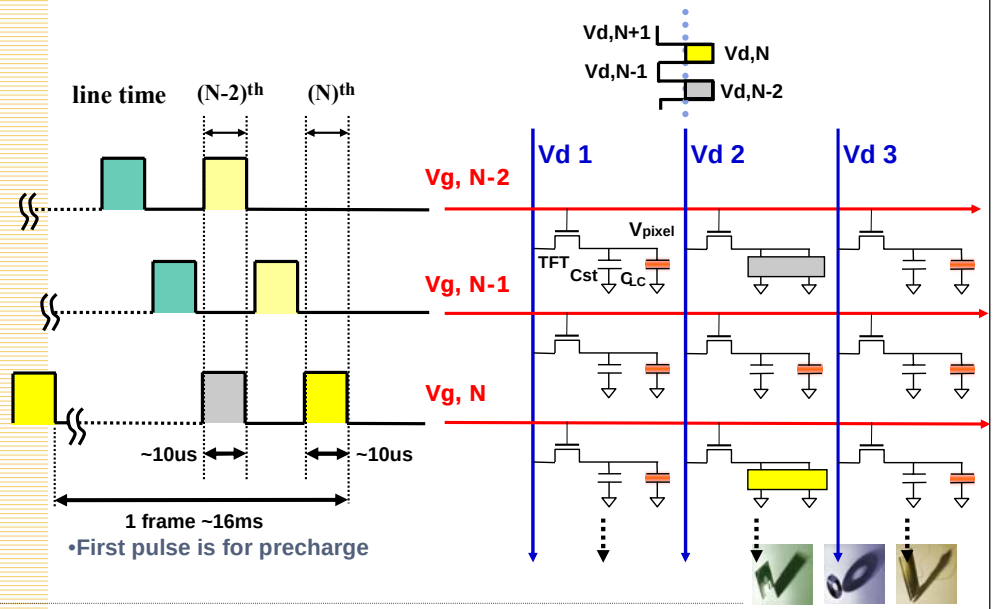
Source : Web of TSMC

Two-Line Scanning

- Frame inversion
- column inversion
- row inversion
- dot inversion



Two-Line Scanning



•First pulse is for precharge

Scan Driver Consideration

Dual Driving

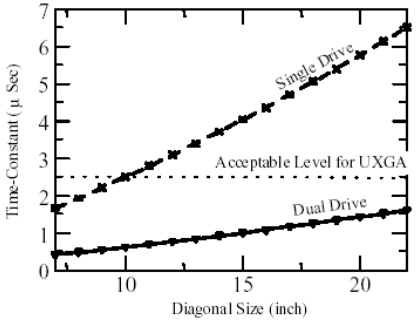


Figure 1. Relationship between Panel Size and Scan-Line-Time-Constant

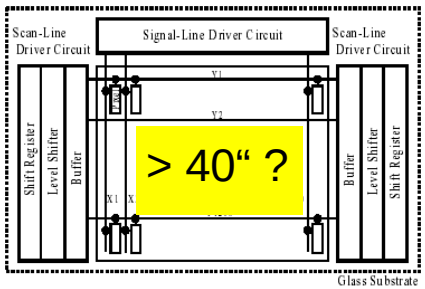


Figure 2. Circuit Construction of the 15-inch UXGA Poly-Si TFT-LCD

The scan driver with both side driving effectively reduces the RC time constant of the gate line.

Ref:IDW 00’, p.167

Gate Driver Design

Toshiba 15” UXGA

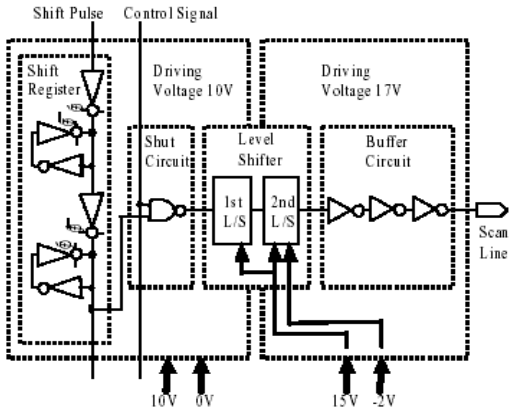


Figure 3. Circuit Diagram of Scan-Line Driver

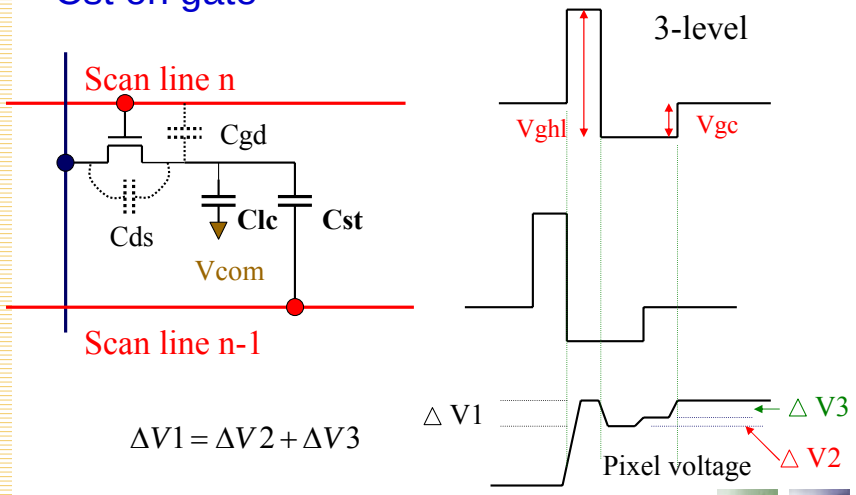
Shut circuit was inserted between S/R outputs and L/S inputs to avoid over current phenomena due to timing difference between right and left side scan driver outputs.

Level shifter is divided in two stages. First stage is made to shift high level from 10 V to 15 V, second stage is made to shift low level from 0 V to –2 V..

Ref:SID 00’, p.1121

Three-level Capacitive Coupling Driving (C. C. Driving)

- Cst on gate



$$\Delta V1 = \Delta V2 + \Delta V3$$

Three-level C. C. Driving

$$\Delta V1 = Vghl \times \frac{Cgd}{Clc + Cst + Cgd + Cds}$$

$$\Delta V2 = Vgc \times \frac{Cst}{Clc + Cst + Cgd + Cds}$$

$$\Delta V3 = Vgc \times \frac{Cgd}{Clc + Cst + Cgd + Cds}$$

Considerpreviouscase,

$$\Delta V_{gd} = \frac{0.05 \times 25}{0.4 + 0.4 + 0.05} = 1.47V$$

$$V_{gc} = \Delta V_{ghl} \times \frac{C_{gd}}{C_s + C_{gd}} = 25\frac{0.05}{0.4 + 0.05} = 2.778$$

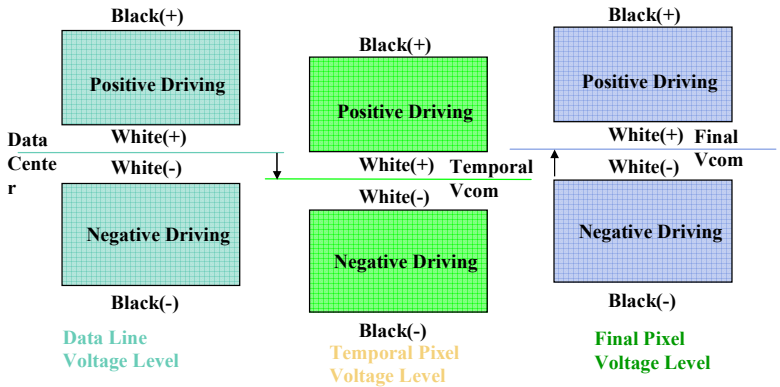
If $\Delta V1 = \Delta V2 + \Delta V3$ i.e. $Vghl \times Cgd = Vgc \times (Cst + Cgd)$

$$Vgc = Vghl \times \frac{Cgd}{Cst + Cgd}$$, then

- Feed-through effect is eliminated.

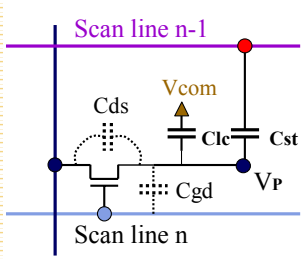
Three-level C. C. Driving

- ***Cs on Gate with 3-Level Driving Scheme***



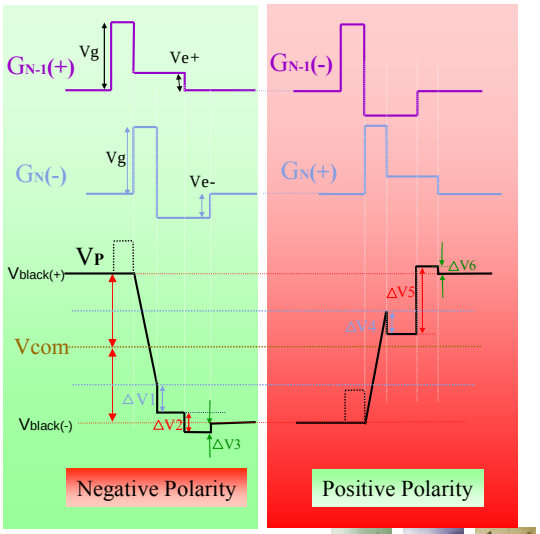
Four-level C. C. Driving

Cs on gate



- **line inversion**
- **low voltage source driver**
- **complex scan driver**

Not valid for Vcom AC



Four-level C. C. Driving

$$\Delta V1 = (Vg + (Ve-)) \times \frac{Cgd}{(Cst + C_{LC} + Cgd)} \qquad \Delta V4 = (Vg - (Ve+)) \times \frac{Cgd}{(Cst + C_{LC} + Cgd)}$$

$$\Delta V2 = (Ve+) \times \frac{Cst}{(Cst + C_{LC} + Cgd)} \qquad \Delta V5 = (Ve-) \times \frac{Cst}{(Cst + C_{LC} + Cgd)}$$

$$\Delta V3 = (Ve-) \times \frac{Cgd}{(Cst + C_{LC} + Cgd)} \qquad \Delta V6 = (Ve+) \times \frac{Cgd}{(Cst + C_{LC} + Cgd)}$$

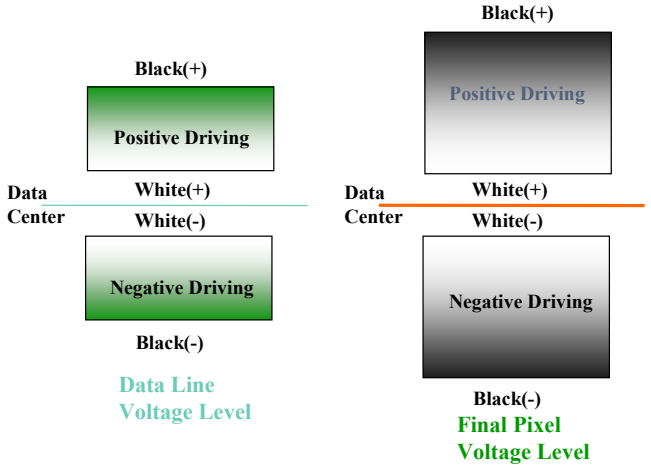
$$\because \Delta V1 + \Delta V2 - \Delta V3 = -\Delta V4 + \Delta V5 - \Delta V6$$

$$\therefore (Ve-) - (Ve+) = 2Vg \times \frac{Cgd}{Cst}$$

- **Pixel voltages of positive polarity and negative polarity for LC cell are symmetry.**

Four-level C. C. Driving

- ***Cs on Gate with 4-Level Driving Scheme***



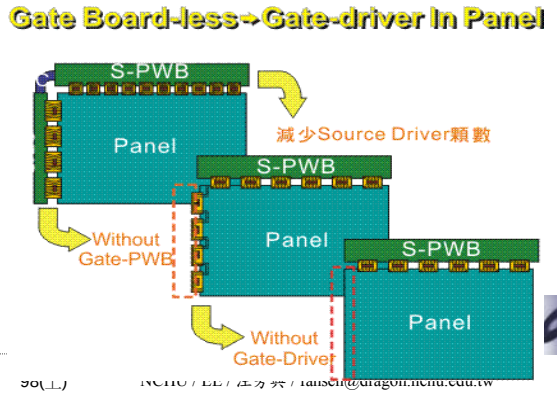
Comparison of Addressing

	Frame	Row	Column	Dot
Common voltage	AC/DC	AC/DC	DC	DC
Output range	Low/high voltage	Low/high voltage	high voltage	high voltage
2-level driving	V	V	V	V
3-level driving	X / V	X / V	V	V
4-level driving	X / V	X / V	X	X

Vcom AC/DC

Trend of Gate Driver IC

- package ：
  - TCP（Tape Carrier Package）→
  - COG（Chip on Glass）→
  - COF （Chip on Film）→
  - GIP（Gate-Driver In Panel）。



Gate-Driver In Panel

Ch4. Driving Circuits Design of A-Si TFT

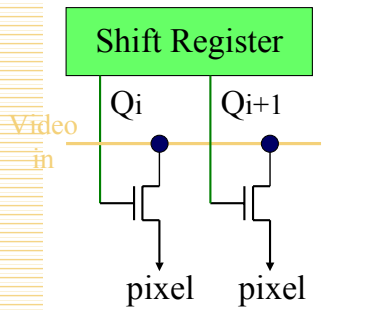
- Gate Driving Circuit
- Source Driving Circuit
  - Driver Architectures
  - Driver Specifications
  - DAC
  - Output Buffer
  - Low power consumption
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface

Source Driver Circuits

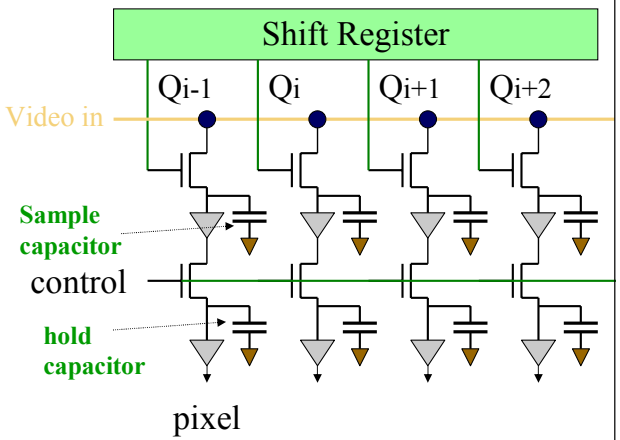
- Also Called Column Driver (Data Driver)
- Driver Architectures
  - Line-at a-time (LAAT)
  - Point-at a-time (PAAT)
- Data Drivers Types
  - Analog Data Driver
  - Digital Data Driver

Analog Data Driver

- Serial In, Serial Out
- Serial In, Parallel Out



Shorter charging time

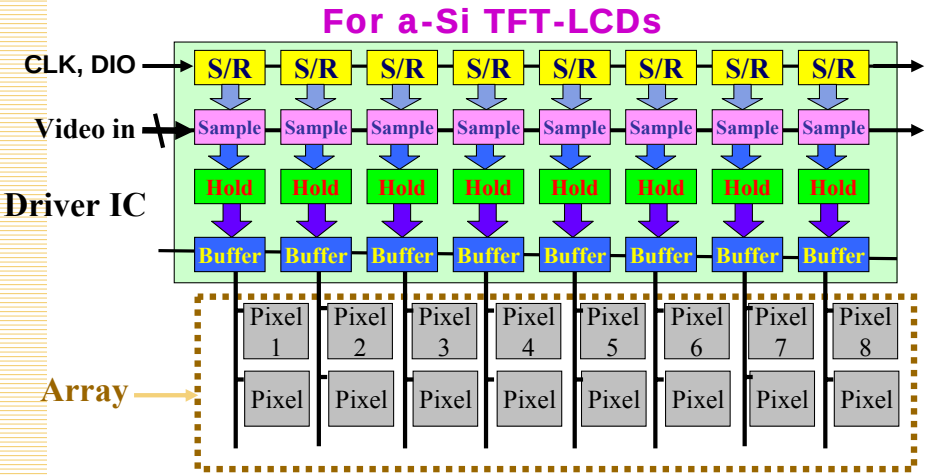


Comparison of Analog Data Driver

	SISO 1 phase	SIPO 1 phase
Circuits complexity	lowest	higher
Pixel charging time	T_{VL} / Pix-H	T_{VL}
Sample time	T_{VL} / Pix-H	T_{VL} / Pix-H
S/R frequency	1/(T_{VL} / Pix-H)	1/(T_{VL} / Pix-H)
Reformed video needed	No	No

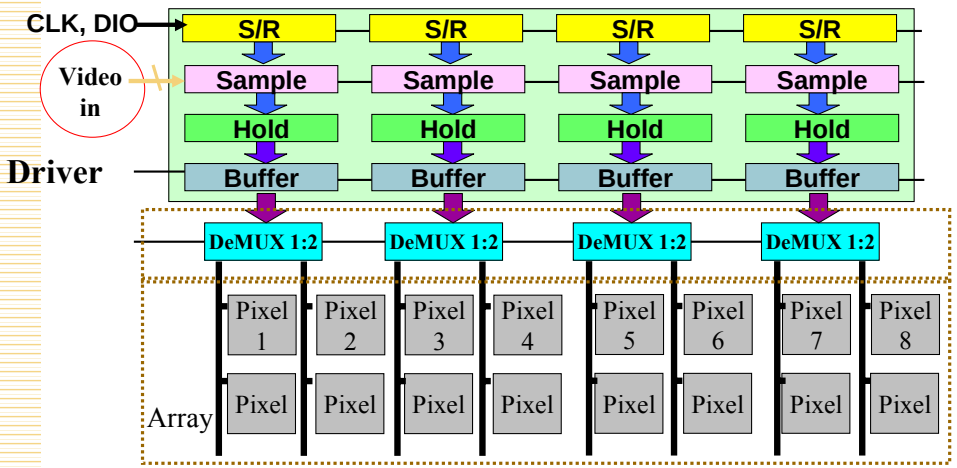
T_{VL} :vertical line time, Pix-H :horizontal pixel number

LAAT Driver Architecture



All video signals stored in A latches are written to B latches simultaneously in each horizontal scanning period. Features: (1) has sufficient charging capability; (2) very difficult to achieve good uniformity of output voltages of the analog buffer.

PAAT Driver Architecture



A high speed and wide voltage range analog interface circuit that consumes a large amount of power is required !! Feature : (1) less data driver ICs ; (2) shorter pixel charging time than LAAT.

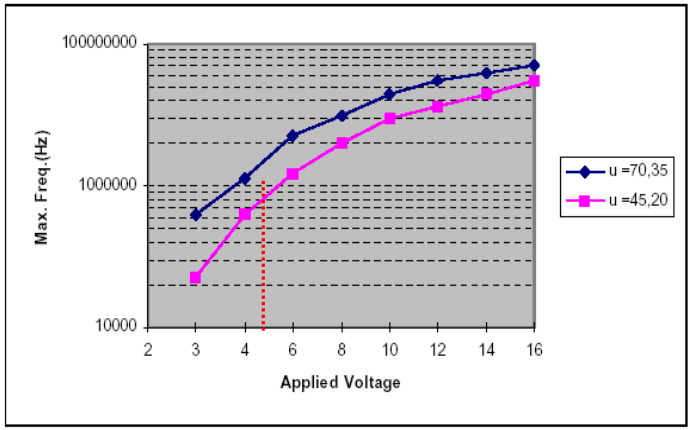
LAAT vs. PAAT

Units	Size Inches	Resolution	Frequency MHz	Technique	Multiplex	Gray Scale Bits
Fujitsu	3.2		6.3	PAAT		
LG		XGA		LAAT		6
Mitsubishi	4		2.5	LAAT		
Sanyo	2	800x234		PAAT	8:1	
Sanyo	5.6	920x234		PAAT	4:1	8
Seiko-Epson	2.9	QVGA	12.5	LAAT		8
Sharp	3.7		6.5			
Sharp	2.2		2.4			
Sharp	3.7		3.15			
Sharp	2.6*	HDTV	13.8			
Toshiba	4	XGA		LAAT		8

* CGS

- **Sanyo has been selling products using the PAAT technology. Since small-size panels have only 234 scan line, there is sufficient time to use PAAT technology.**
- **Seiko-Epson has adopted the LAAT architecture because there studies indicated that the crosstalk on a multiplexed circuit was too severe.**

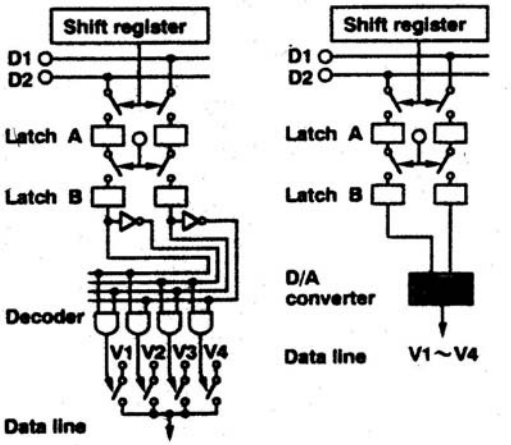
Max. Frequency of Shift Registers



Vcc=5V, Freq.<2MHz @ $\mu_{n/p}$=70/35 cm²/Vs

Ref:SID'96 Digest. pp.673.

Digital Data Driver



(a) Decoder type is very difficult to achieve full gray scale because the circuit configuration is too complicated !

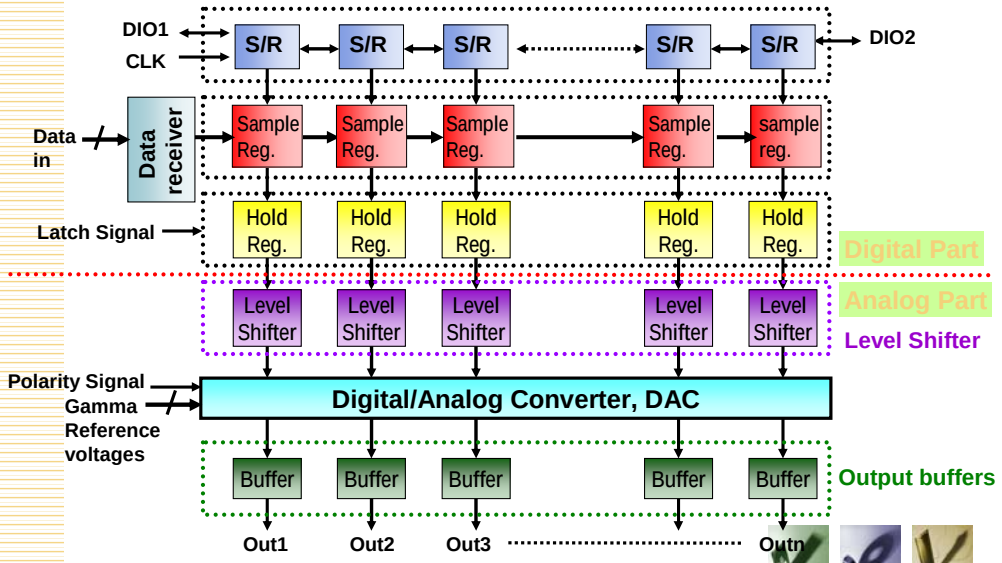
(b) DAC type is the most promising one because it has a less complicated configuration while keeping full digital interface !

Ref:IDW 00' p.171

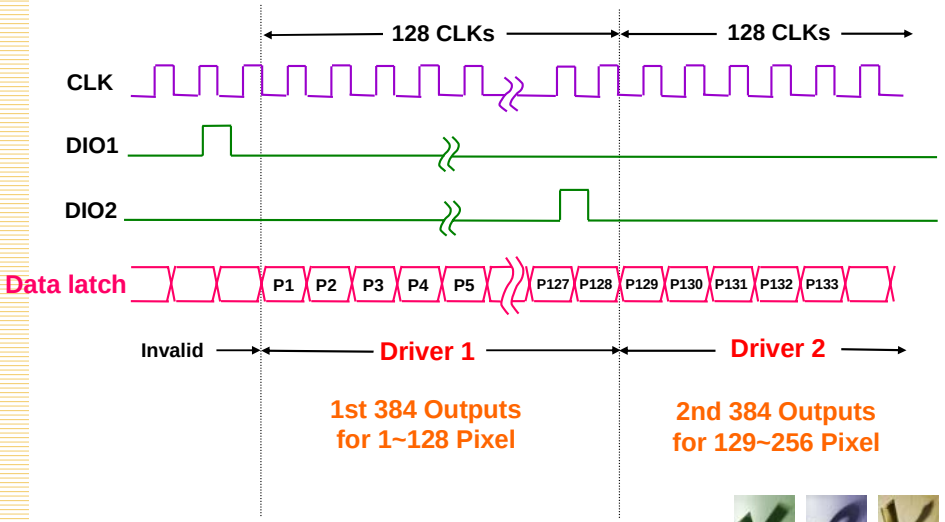
Comparison of Digital/Analog Data Driver

	Digital	Analog
circuits complexity	complex	simple
noise immunity	high	low
gamma correction	Yes	No
video signal processing	Compatible to PC	ADC needed
cost	high	low

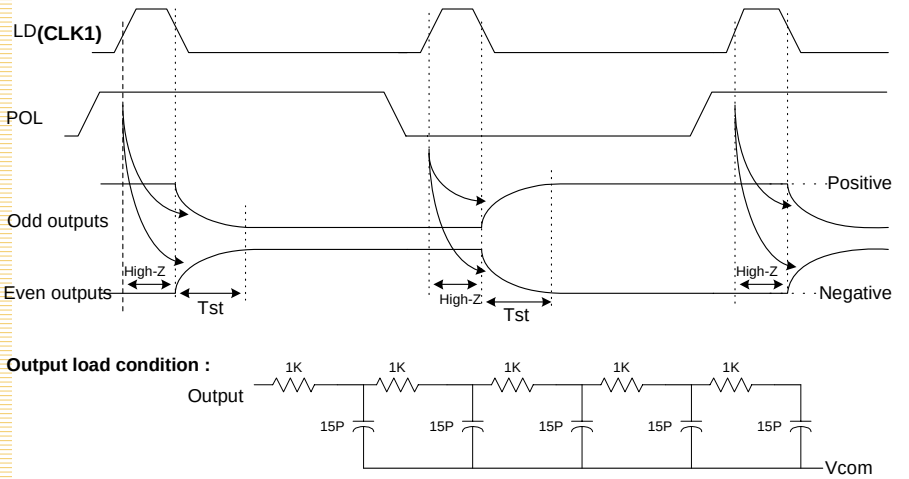
Architecture of Source Driver IC for Large-Size TFT-LCDs



Timing Diagram of Source Driver



Timing Diagram of Source Driver



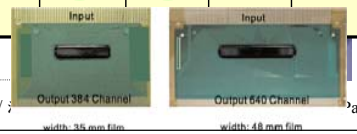
Key Specifications

- Channel number (384, 402, 420, 480, 640, 720…)
- Gray scale (6 bit, 8 bit, 10 bit…)
- Max operation frequency (45MHz, 55MHz, 65MHz, 75MHz…)
- Pixel charging time (eg. R=2k, C=20pF, 6.5us 90%, 11.5us 99.9%)
- Frame/row/column/dot inversion
- Output voltage deviation (±20mV, ±10mV, ±5mV, ±3mV)
- Output voltage (10V, 12V, 13.5V, 15V, 18V)
- Interface (TTL, RSDS, mini-LVDS)
- Operation voltage (2.5V, 3.3V)
- No. of Gamma reference voltage (10, 14, 18)
- Package (TCP, COG, COF)
- Others (data inversion, low-power mode, offset canceling, charge sharing …etc.)

Channel Number vs. Resolution

- Source driver : No. of driver and No. of output channel

	No. of lines	12	10	9	8	7	6	5
VGA	640x3		192		240			384
SVGA	800x3		240		300		402	480
XGA	1024x3		312		384			
SXGA,WXGA	1280x3		384		480		640	
WXGA	1366x3		414					
SXGA+	1400x3		420					
WXGA	1440x3		432	480				
UXGA	1600x3	402	480					
WSXGA+	1680x3	420				720		
HDTV	1920x3	480		642	720			
QXGA	2048x3	512						



Resolution vs. Max. Frequency

Frame rate	60 Hz	60 Hz	75 Hz	75 Hz
	Pixel frequency	Horizontal period	Pixel frequency	Horizontal period
VGA	25.2 MHz	31.7 μs	31.5 MHz	26.7 μs
SVGA	40 MHz	26.4 μs	49.5 MHz	21.3 μs
XGA	65 MHz	20.7 μs	78.75 MHz	16.7 μs
SXGA	108 MHz	15.6 μs	135 MHz	12.5 μs
UXGA	162 MHz	13.3 μs	202.5 MHz	10.7 μs

Higher resolution, shorter pixel charging time, higher driving frequency

D/A Converter

- Fundamentals of Data Converter
- Digital-to-Analog Converters

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Fundamentals of Data Converter

- Ideal D/A converter
- Quantization error in ideal DACs
- Performance limitation
- Offset error
- Gain error
- Accuracy

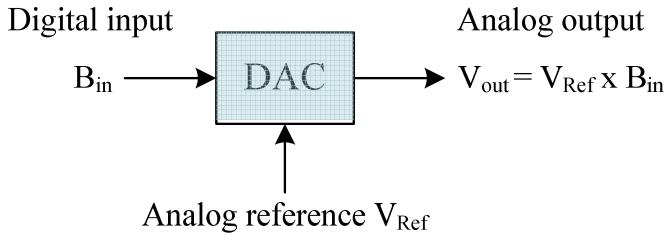
資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Idea D/A Converter

- Ideal N-bit DAC
  - Digital input

$$B_{in} = \frac{b_{n-1}}{2^1} + \frac{b_{n-2}}{2^2} + L + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}$$

Where b_i is 1 or 0, i.e. binary, b_{n-1} is the MSB, and b_0 is the LSB



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Idea D/A Converter (cont')

- Analog output V_{out} is related to B_{in} through an analog reference, V_{Ref}
  1. V_{out} and V_{Ref} may be voltage, current, or charge.
  2. We assume here that they are voltage (for simplicity)
  3. Definitions：

$$V_{out} = V_{ref}\left(\frac{b_{n-1}}{2^1} + \frac{b_{n-2}}{2^2} + L + \frac{b_1}{2^{n-1}} + \frac{b_0}{2^n}\right) = V_{ref} \times B_{in},$$

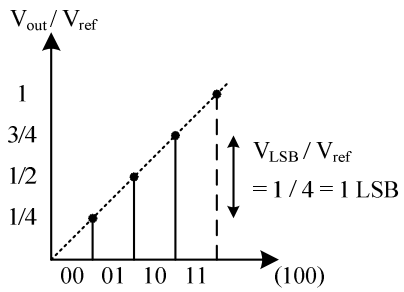
$$V_{LSB} = \frac{V_{ref}}{2^N}$$, where V_{LSB} is defined as the voltage changes when one LSB changes.

- 1 LSB = $1/2^N$ unitless definition.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Idea D/A Converter (cont')

- An ideal 2-bit DAC example：Input-output transfer curve. In general, the maximum value of V_{out} is not V_{Ref} but rather $V_{Ref}(1-2^{-n})$ or equivalently, V_{Ref}-V_{LSB}.



- A multiplying DAC (MDAC) is realized by simply allowing the reference signal, V_{REF}, to be a varying input signal along with B_{IN}. Such an arrangement results in Vout being proportional to the multiplication of the input signals, B_{IN} and V_{Ref}.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Quantization Error in DACs

- ***Quantization error*** (noise) is the inherent uncertainty in digitizing an analog value with a finite resolution converter. It is equal to the analog output of the infinite-bit DAC minus that of the finite-bit DAC.

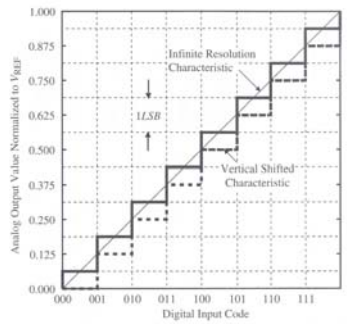


Figure 10.1-4 Ideal input–output characteristics of a 3-bit DAC.

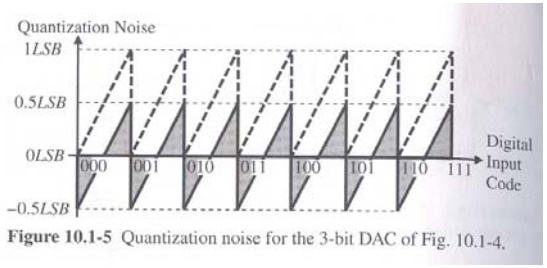


Figure 10.1-5 Quantization noise for the 3-bit DAC of Fig. 10.1-4.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Performance Limitation

- Definitions for determining the transfer responses for DACs.
  - The transfer response of a DAC is defined to be the analog levels that occur for each of the digital word.
- Resolution
  - The number of distinct analog levels corresponding to different digital words. Thus, an N-bit resolution implies that the converter can resolve 2^N distinct analog levels.

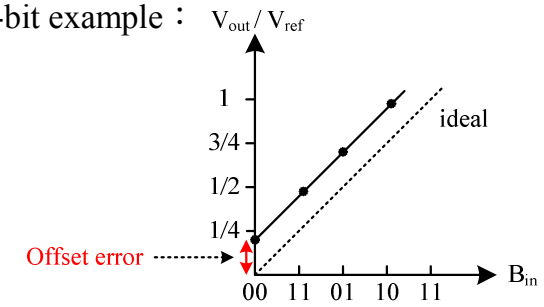
資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Offset Error

- Offset error is in units of LSBs.
- Offset error is the output that occurs for the input code that should produce zero output.

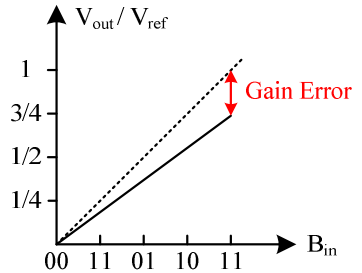
$$E_{off}(DAC) = V_{out}/V_{LSB}\Big|_{0...0}$$

- 2-bit example：



Gain Error

- Gain error is the difference at the full-scale value between the ideal and actual when the offset error has been reduced to zero.
- Gain error is in units of LSBs.
- DACs：
  - $E_{gain(DAC)} = \left(V_{out}/V_{LSB}\Big|_{1...1} - V_{out}/V_{LSB}\Big|_{0...0} \right) - (2^N - 1)$
  - 2-bit example：



Accuracy

- Absolute accuracy
  - The difference between the expected and actual and transfer response.
  - Includes 1.offset error, 2. gain error, 3. linearity error
- Relative accuracy
  - The accuracy of offset and gain errors have been removed

Accuracy (cont')

- Accuracy can be expressed as a percentage error of full-scale value, as the effective number of bit, or as a fraction of an LSB.
  - For example, a 12-bit accuracy implies that the converter's error is less than the full-scale divided by 2^{12}.
  - A converter may have 12-bit resolution with only 10-bit accuracy, or 10-bit resolution with 12-bit accuracy.
  - An accuracy greater than the resolution means that the converter's transfer response is very precisely controlled. (better than the number of bits of resolution)

D/A Converter

- Fundamentals of Data Converter
- Digital-to-Analog Converters

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC
- Binary-weighted converters
- Glitches
- Thermometer-code DACs

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Nyquist-rate D/A converters

- Four main types
  - ✓ Decoder-based
  - ✓ Binary-weighted
  - ✓ Thermometer-code
  - ✓ Hybrid

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Decoder-Based DAC

- Most straight forward approach
  - Create 2^N reference signals and pass the appropriate signal to the output.
- Three main types：
  - Resistor string
  - Folded resistor-string
  - Multiple resistor-string

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Decoder-Based DAC

- Most straight forward approach
  - Create 2^N reference signals and pass the appropriate signal to the output.
- Types：
  - ***Resistor string***
  - Folded resistor-string

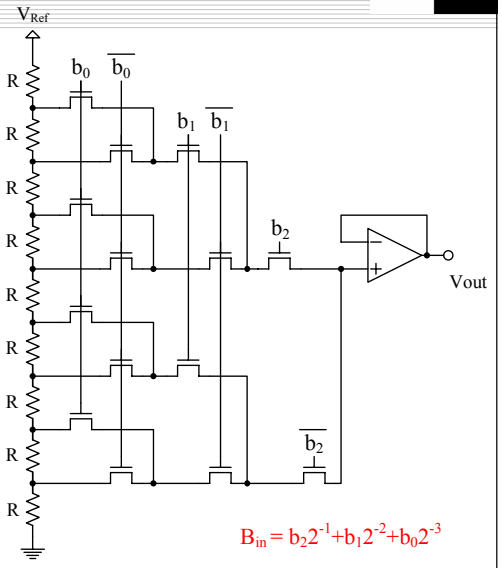
資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Resistor-string DAC

- Example 1：a 3-bit DAC with transmission gate, *tree-like* decoder.

- Transmission gates might be used rather than n-channel switches.

- Extra drain and source capacitance (to GND) is offset by the reduced switch resistance.
- Larger layout
- Can operate closer to positive supply voltage.



$B_{in} = b_2 2^{-1} + b_1 2^{-2} + b_0 2^{-3}$

2^N resistors

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Resistor-string DAC (cont')

- Only n-channel switches are used
  1. About the same speed as the transmission gate implementation.
  2. Compact layout (no contacts are required in the tree)
- Monotonicity is guaranteed (if the buffer's offset does not depend on its input voltage)
- The accuracy of this DAC depends on the type of resistor uesd. Polysilicon (20-30 Ω/□) can have up to 10 bits of accuracy.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Resistor-string DAC (cont')

- Speed
  - Can be estimated using open-circuit time-constant approach (refer to microelectronics textbook written by Sedra and Smith)
  - Time-constant

$$\approx 3R_{tr}C_{tr} + 2\cdot 3R_{tr}C_{tr} + \cdots + N\cdot 3R_{tr}C_{tr}$$

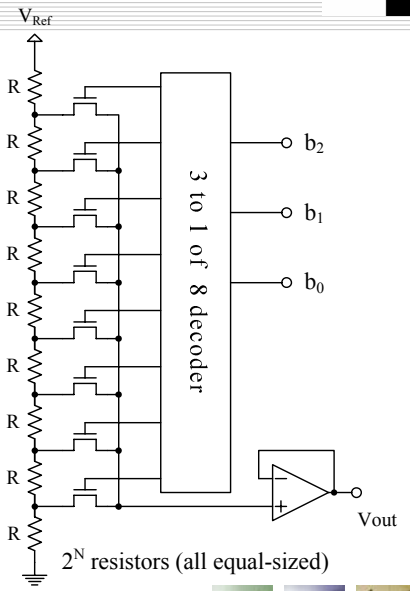
$$= N(N+1)/(2\cdot 3R_{tr}C_{tr})$$

Where R_{tr} is on resistance of switches,
C_{tr} is drain or source capacitance of switches, and
N is bit number.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Resistor-string DAC (cont')

- **Example 2**：a 3-bit DAC with digital decoding.
  - Compared to example1：
    1. Higher speed
    2. More area for decoding circuit
  - Speed
    - Time-constant ≈$R_{tr}\cdot 2^N C_{tr}$
    - For N≦6 example 2 is faster
    - For N>7 example 1 is faster
- Compromise between example 1 and example 2.
  - ➢ Folded resistor-string DAC

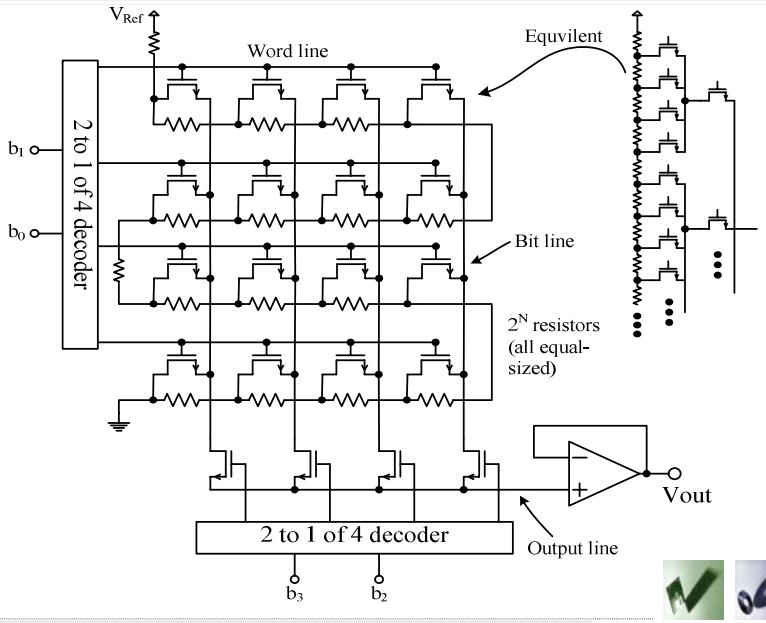


資料來源：林克見, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Decoder-Based DAC

- Most straight forward approach
  - Create 2^N reference signals and pass the appropriate signal to the output.
- Types：
  - Resistor string
  - ***Folded resistor-string***

Folded resistor-string DAC



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
蘇育民, "數位類比轉換器設計與測試之研究," 暨南國際大學電機工程學系碩士論文, 2004

Folded resistor-string DAC (cont')

- Reduced the amount of digital decoding
- Reduce large capacitive loading
- Decoding is very similar to that for a digital memory
- Example：
  - 4 bit (2 bit+2 bit) DAC
  - Time constant ≈ $Rtr\cdot(2^2C_{tr})+2R_{tr}\cdot(2^2C_{tr})$
- Other design examples：
  - 12 bit = 6 bit + 6 bit, or 4 bit + 4 bit + 4 bit, or ……
  - 10 bit = 5 bit + 5 bit, or 3 bit + 3 bit + 4 bit, or ……

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
蘇育民, "數位類比轉換器設計與測試之研究," 暨南國際大學電機工程學系碩士論文, 2004

Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC
- ***Binary-weighted converters***
- Glitches
- Thermometer-code DACs

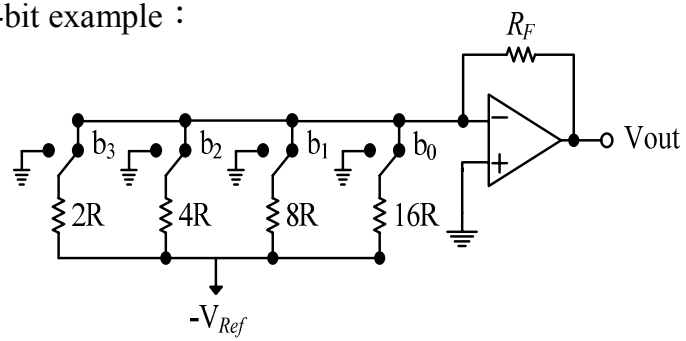
Binary-Weighted (or Binary-Scaled) Converter

- An appropriate set of signals that are all related in a binary fashion
- The binary array of signals might be voltages, charges, or currents.
- Five main types：
  - Binary-weighted resistor DAC
  - Reduced-resistor-ratio ladders
  - R-2R-based DAC
  - Charge-redistribution switched-capacitor DAC
  - Current-mode DAC

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克兒, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.
蘇育民, "數位類比轉換器設計與測試之研究," 暨南國際大學電機工程學系碩士論文, 2004

Binary-Weighted Resistor DAC

- 4-bit example：



$$V_{out} = -R_F V_{ref}\left(-\frac{b_3}{2R}-\frac{b_2}{4R}-\frac{b_1}{8R}\right)=\left(\frac{R_F}{R}V_{ref}\right)B_{In}$$

$$where: B_{In} = b_3 2^{-1} + b_2 2^{-2} + b_1 2^{-3} + \cdots\cdots$$

資料來源： Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002, p.624

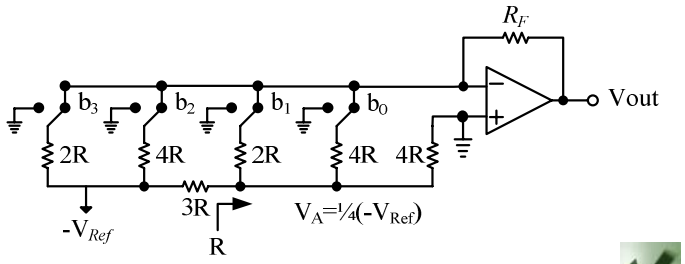
Binary-weighted resistor DAC (cont')

- Does not require many resistors or switches.
- Disadvantage
  1. Resistor ratio and current ratio are on the order of 2N. If N is large, this large current ratio requires that the switches also be scaled so that equal voltage drops appear them.
  2. Monotonicity is no guaranteed.
  3. Prone to glitch.

資料來源： Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002, p.624

Reduced-resistor-ratio Ladders

- Reduce the large resistor ratios in a binary-weighted array
- Introduce a series resistor to scale signals in portions of the array
  - Ex : $V_A = -1/4 V_{Ref}$



資料來源:林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

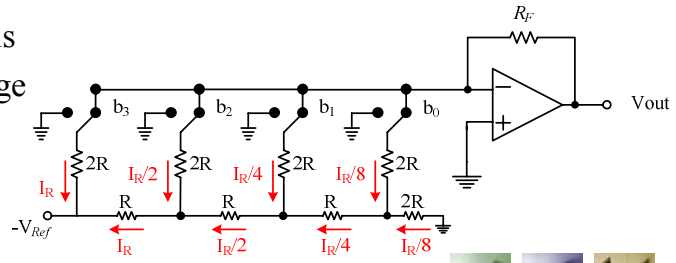
Reduced-resistor-ratio Ladders (cont')

- An additional 4R was added such that resistance seen to right of the 3R equals R.
- One-fourth the resistance ratio compared to the binary-weighted case.
- Current ratio has remained unchanged
  - Switches must be scaled in size.
- Repeating this procedure recursively, one can obtain an R-2R ladder.

資料來源：林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

R-2R-based DAC

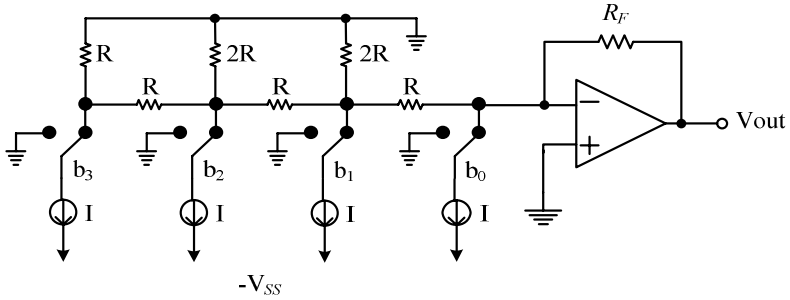
- Smaller size and better accuracy than a binary-sized approach
  - Small number of components
  - Resistance ratio of only 2
- 4-bit example： $I_R = \frac{V_{ref}}{2R}, and\ \_V_{out} = R_F \cdot \sum_{i=1}^{N} \frac{b_i \cdot I_R}{2^{i-1}} = V_{ref} \cdot \left(\frac{R_F}{R}\right) \sum_{i=1}^{N} \frac{b_i}{2^i}$
- Current ration is still large→ large ratio of switch sizes



資料來源： Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002, p.625

R-2R-based DAC (cont')

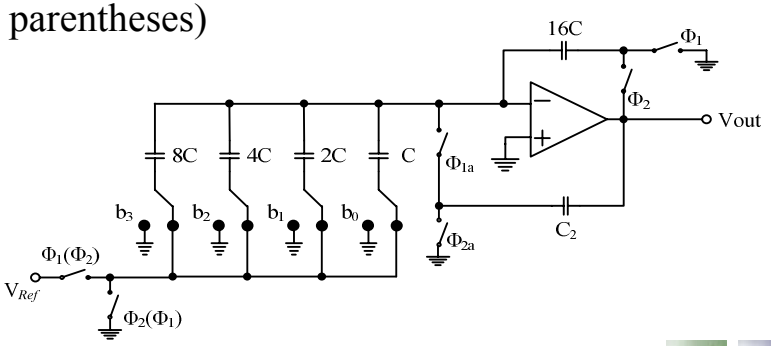
- R-2R ladder DAC with equal currents through switches
- Slower since the internal nodes exhibit some voltage swings (as opposed to the previous configuration where internal nodes all remain at fixed voltage).



資料來源：呂學旺, "場發射顯示器驅動電路之設計," 國立交通大學電子工程學系碩士論文, 1994.
魯得中, "場效激發元件驅動器的設計," 國立交通大學電子工程學系碩士論文, 2003.

Charge-redistribution switched-capacitor DAC

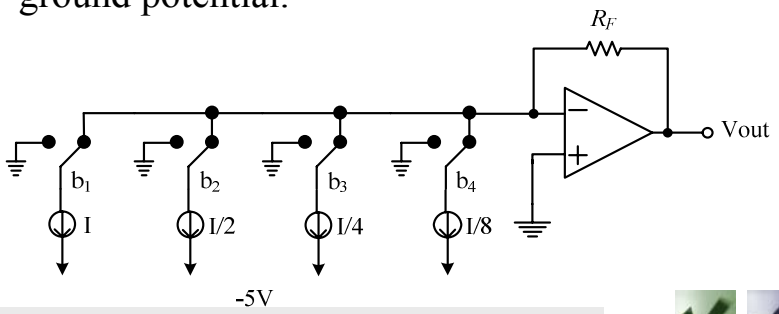
- Insensitive to Op Amp input-offset voltage, 1/f noise, and finite amplifier gain.
- An additional sign bit can be realized by interchanging the clock phases (shown in parentheses)



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.

Current-mode DAC

- High-speed
- Switch current to output or to ground
- The output current is converted to a voltage through R_F.
- The upper portion of current source always remains at ground potential.



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

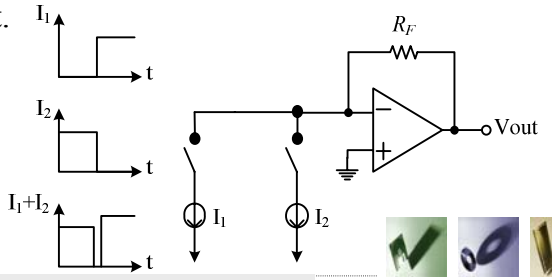
Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC
- Binary-weighted converters
- ***Glitches***
- Thermometer-code DACs

Glitches

- A major limitation during high-speed operation
- Mainly the result of different delays occurring when switching different signals
- Example：01111……1→1000……0

1. I_1 represents the MSB current and I_2 represents the sum of (N-1) LSB currents.
2. The MSB current turns off slightly early, causing a glitch of zero current.



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.

Glitches (cont')

- Glitch disturbance can be reduced by：
  1. Limiting the bandwidth (placing a capacitor across RF)
  2. Using a sample and hold on the output signal.
  3. Modifying some or all of the digital word from a binary code to a thermometer code.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.

Digital-to-Analog Converters

- Nyquist-rate D/A converters
- Decoder-based DAC
- Binary-weighted converters
- Glitches
- ***Thermometer-code DACs***

Thermometer-Code DAC

- Digital recode the input to a thermometer-code equivalent.

Thermometer-code representations for 3-bit binary values

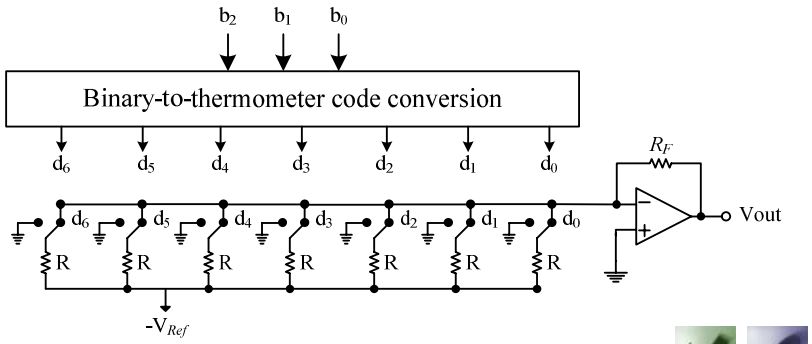
Decimal	Binary			Thermometer Codes						
	b_1	b_2	b_3	d_1	d_2	d_3	d_4	d_5	d_6	D_7
0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	1
2	0	1	0	0	0	0	0	0	1	1
3	0	1	1	0	0	0	0	1	1	1
4	1	0	0	0	0	0	1	1	1	1
5	1	0	1	0	0	1	1	1	1	1
6	1	1	0	0	1	1	1	1	1	1
7	1	1	1	1	1	1	1	1	1	1

- Advantages over its binary-weighted counterpart
  1. Low DNL errors
  2. Guaranteed monotonicity
  3. Reduced glitching noise
- Does not increase the size of the analog circuitry compared to a binary-weighted approach.

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Thermometer-Code DAC (cont')

- Total area required by the transistor switches is the same.
- All transistor switches are of equal sizes since they all pass equal currents.
- Example： Thermometer-code resistor DAC



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

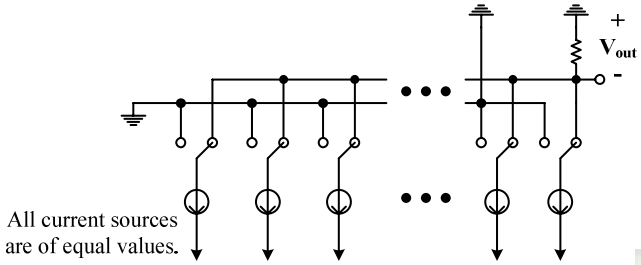
Thermometer-Code Current-Mode DAC

- Row and column decoders
- Inherent monotonicity
- Good DNL errors
- INL errors depend on the placement of the current sources

資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Thermometer-Code Current-Mode DAC (cont')

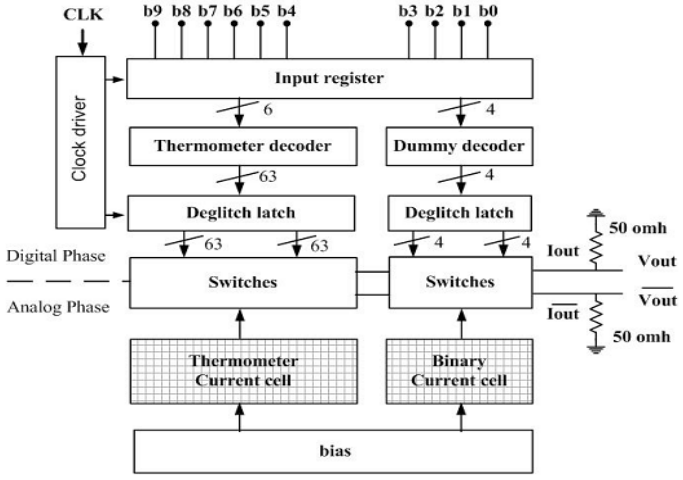
- In high-speed applications
  1. The output current feeds directly into an off-chip 50Ω or 75Ω resistor, rather than an output opamp.
  2. Cascode current sources are used to reduce current-source variation due to voltage changes in V_{out}.



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

Examples of DAC 1

- Chun-Yueh Huang; Tsung-Tien Hou; Hung-Yu Wang; "**A 10 bit 100-MHz current-steering DAC**" ASIC, 2005. ASICON 2005. 6th international Conference On Volume 1, 24-0 Oct. 2005 Page(s):411 - 414



Examples of DAC 2.

12-bit DAC Paper- A Novel Linear Digital-to-Analog Converter using Capacitor coupled Adder for LCD Driver ICs

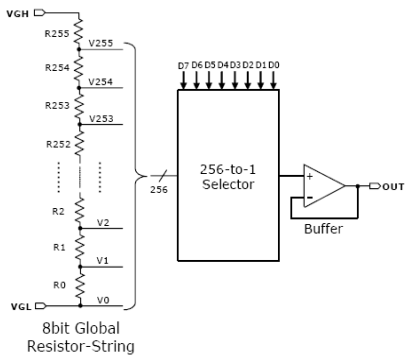


Figure 1 Block diagram of the 8bit Resistor-String DAC.

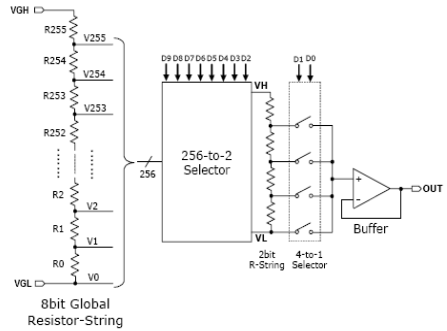


Figure 2 Block diagram of the 10bit Resistor-Resistor String DAC (RR-DAC).

Examples of DAC 3

- 12 Bit Linear DAC using capacitor coupled adder

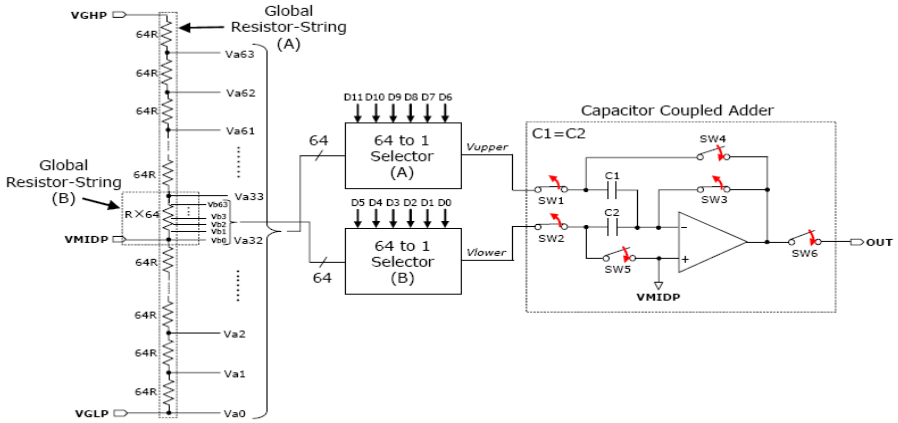
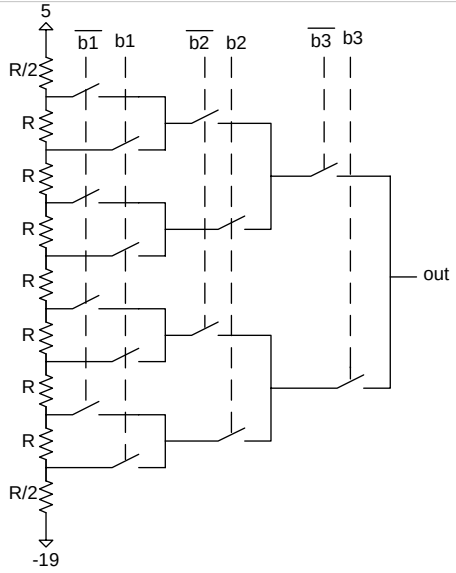


Figure 3 Proposed 12bit linear DAC using capacitor coupled adder

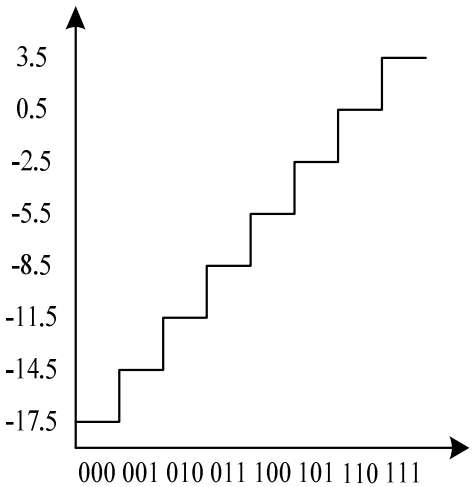
R-String DAC



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

R-String DAC (cont')

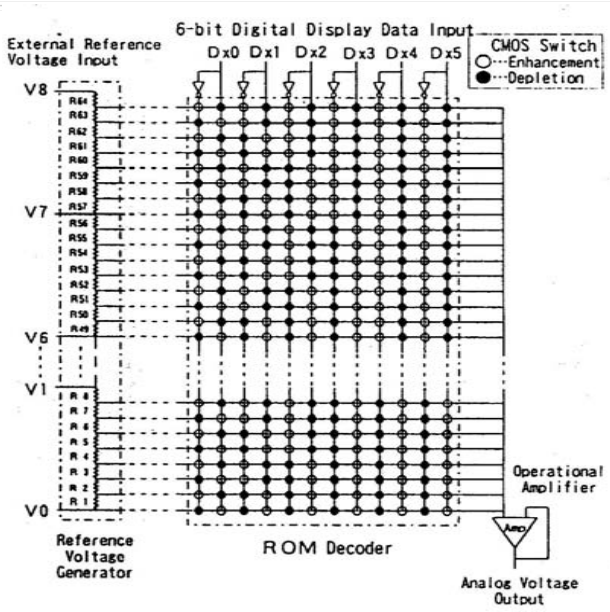
b3	b2	b1	
0	0	0	3.5
0	0	1	0.5
0	1	0	-2.5
0	1	1	-5.5
1	0	0	-8.5
1	0	1	-11.5
1	1	0	-14.5
1	1	1	-17.5



資料來源：Philip E. Allen, Douglas R. Holberg, "CMOS analog circuit design", *Oxford*, 2002.
林克晃, "ADC及DAC積體電路實作," MSD聯盟-混合訊號式積體電路設計技術推廣教育計畫.

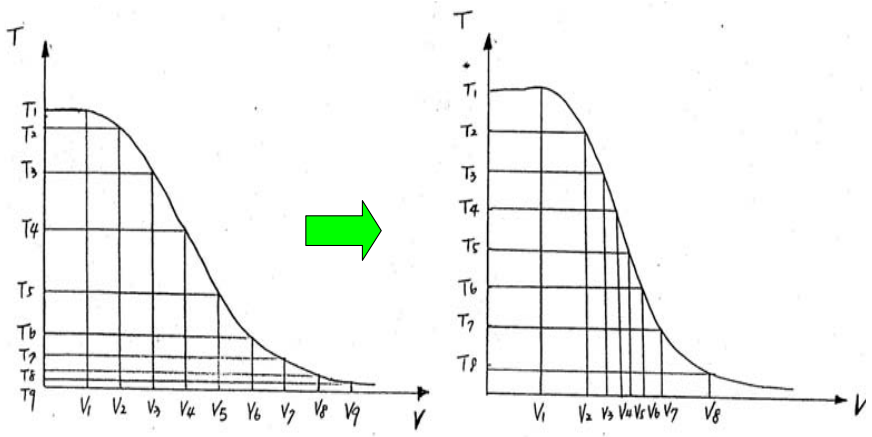
D/A Converter of Source Driver IC

DAC with ROM Decoder



Gamma Correction

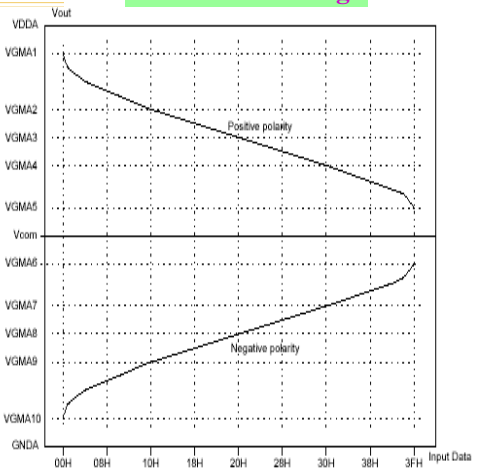
T-V curve is non-linear.



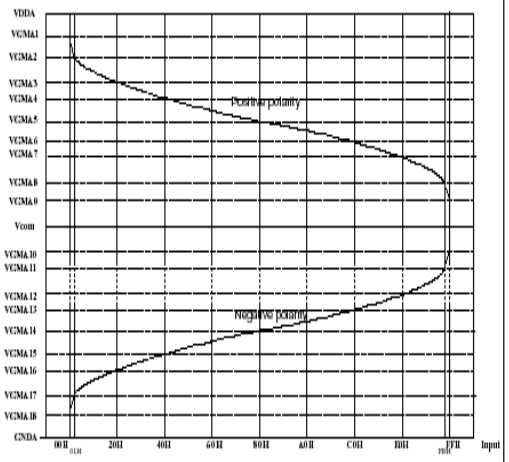
Adjust the voltage of V1~V8 to obtain the desire transmittance.

Gamma Correction

10 Gamma Voltage



18 Gamma Voltage



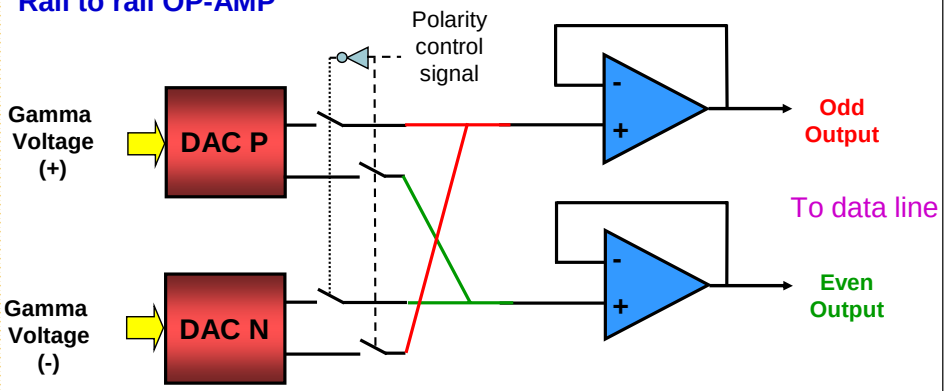
資料來源： Datasheet of Novetek Corp.

R-String (ROM Decoder) DAC

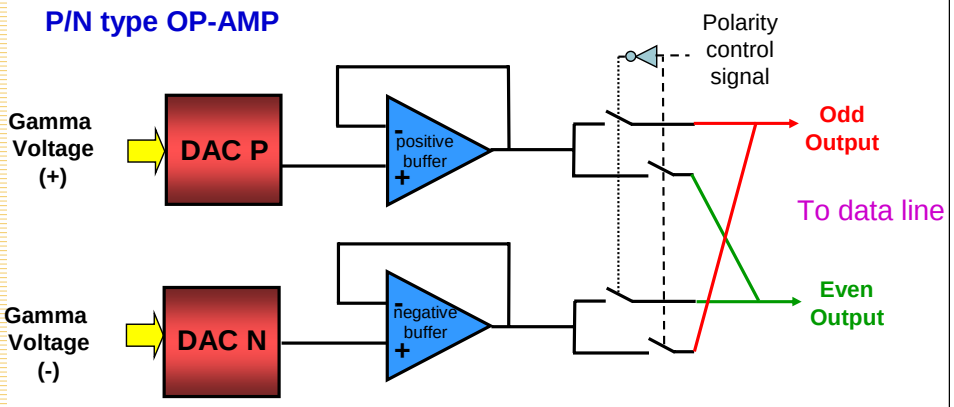
- Advantages
  - Simple architecture
  - Low noise
  - Optimized gamma curve
- Disadvantages
  - Large area
  - Area increase rapidly as bit number increases
  - Steady current consumption in R-string

Output Buffer

Rail to rail OP-AMP

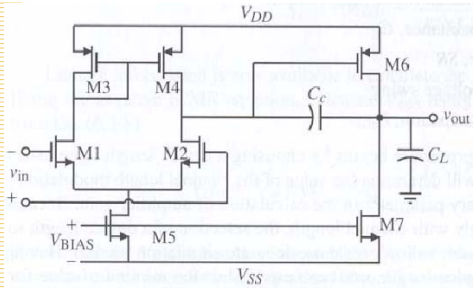


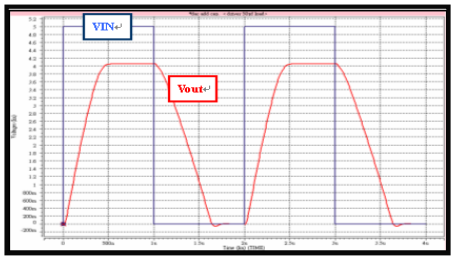
Output Buffer

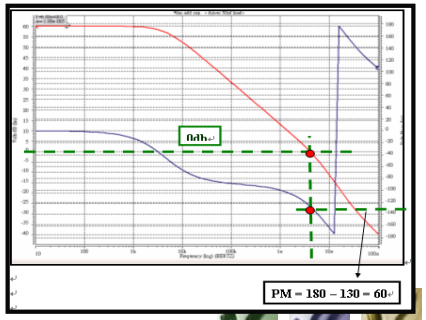


Positive and negative signals are applied by DAC1 and DAC2 separately. Dynamic range of each DAC is reduced to ½ compared with conventional ones.

OP-AMP – An Example



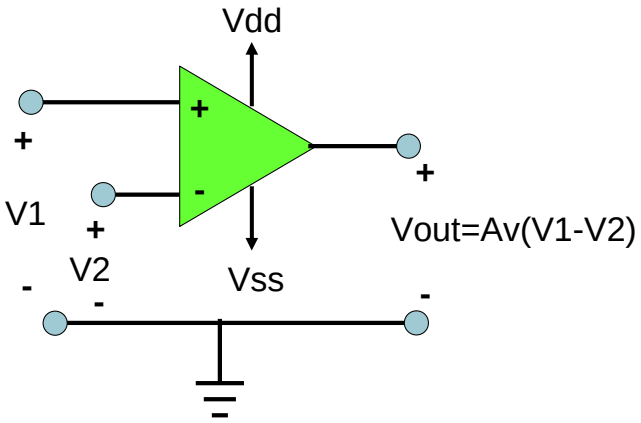




- Wide Dynamic Range (Rail to Rail)
- Low deviation
- High driving ability
- Low power consumption
- Optimum OP AMP. area

Design of Output Amplifier

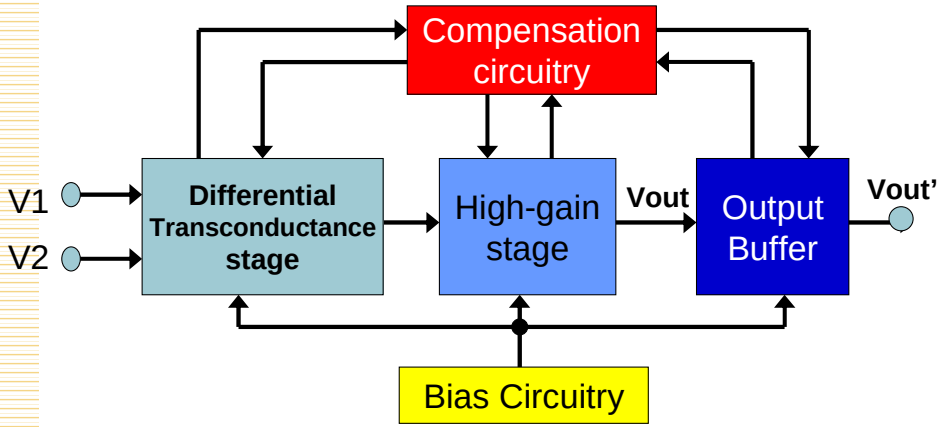
- OP-AMP



Ref: P. E. Allen, D. R. Holberg, “CMOS Analog Circuit Design,” 2nd Ed., Oxford, 2002

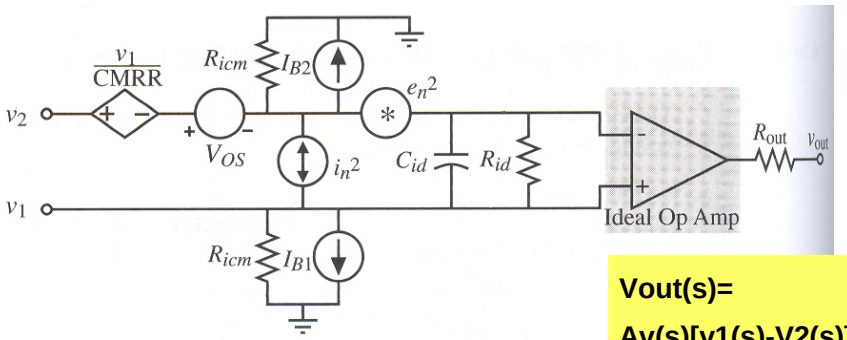
Design of Output Amplifier

- CMOS OP-AMP



Ref: P. E. Allen, D. R. Holberg, “CMOS Analog Circuit Design,” 2nd Ed., Oxford, 2002

Model for a Nonideal Op-Amp



Vout(s)=
Av(s)[v1(s)-V2(s)]
±Ac(s)[v1(s)+V2(s)]/2

- Finite differential-input impedance *Rid, Cid*
- Output resistance *Rout*
- Common-mode input resistance *Ricm*
- Input offset voltage *Vos*
- Input offset current *Ios*=|I_{B1}-I_{B2}|
- Common-mode rejection ratio : *v1*/CMRR
- Noise : i_n^2, e_n^2

Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002

Classification of Op-Amp

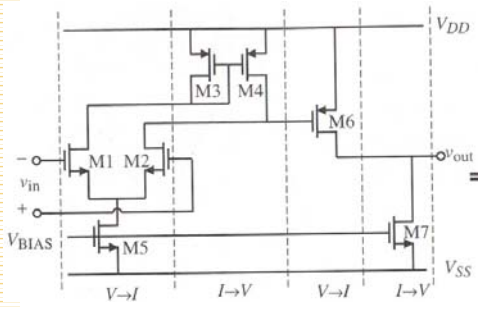
conversion	Hierarchy	
voltage to current	Classic differential amplifier	modified differential amplifier
Current to voltage	Differential-to-single-ended load (current mirror)	Source/sink Current load / MOS diode load
voltage to current	Transconductance grounded gate	Transconductance grounded gate
Current to voltage	Class A (source or sink load)	Class B (push-pull)

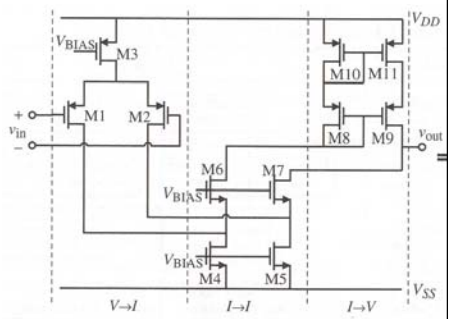
1st voltage stage
Current stage
2nd voltage stage

Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002

Examples of Op-Amp

- Classical two-stage CMOS op amp
- Folded-cascode op amp





Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002

Design of Op Amp

- Procedures
  - Choosing or creating the basic structure
  - Select dc currents and transistor size
  - Boundary conditions
    - Process specification (Vt, k', Cox…)
    - Supply voltage/current and range
    - Operating temperature and range

1. Hand calculation
2. Computer simulation

Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002

Design of Op Amp

Performance requirement	Example
Gain	≧70 db
Gain bandwidth	≧5 MHz
Settling time	≦1 us
Slew rate	≧5 V/us
Input common-mode range, ICMR	≧±1.5 V
Common-mode rejection ratio, CMRR	≧60 db
Power-supply rejection ratio, PSRR	≧60 db
Output voltage swing	≧±1.5 V
Output resistance	N/A
Offset	≦ ± 10 mV
Noise	≦100 nV/√Hz@1 kHz
Layout area	≦ 5000 x (min. L)^2

Model Parameters for a Typical CMOS Bulk Process

Parameter symbol	Process description	Typical parameter value		unit
		n-channel	p-channel	
V_{T0}	Threshold voltage (V_{BS}=0)	0.7±0.15	-0.7±0.15	V
K'	Transconductance parameter (in sat.)	110.0±10%	50.0±10%	uA/V^2
γ	Bulk threshold parameter	0.4	0.57	V$^{1/2}$
λ	Channel length modulation parameter	0.04(L=1um) 0.01(L=2um)	0.05(L=1um) 0.01(L=2um)	V^{-1}
$2\lvert\varphi_F\rvert$	Surface potential at strong inversion	0.7	0.8	V

Model parameters for a typical CMOS bulk process using the simple model with values based on a 0.8um silicon-gate bulk CMOS n-well

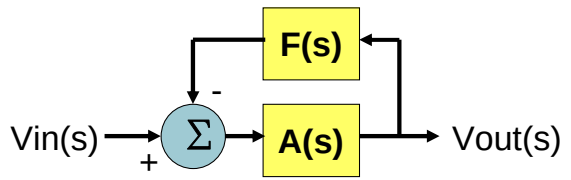
Design of Op Amp

- Procedures
  - Decide on a suitable configuration
    - Trade-off between noise, offset, power…
  - Determine the compensation method
    - Especially for very large C_{LOAD}
  - Design device sizes for proper dc, ac, and transient performance
    - Hand calculation : 80% → important to get a feel for sensitivity of parameter variation
    - computer simulation : 20% → for optimization

Rule: (use of simulator) x (common sense) = constant

Frequency and Phase Response (1/3)

- For a single-loop, negative-feedback system



Stable → $|A(j\omega_{0^\circ})\,F(j\omega_{0^\circ})| = |L(j\omega_{0^\circ})| < 1$

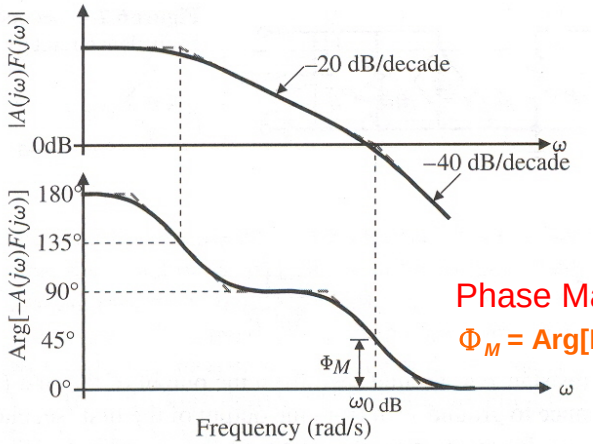
where ω_{0° is defined as $\text{Arg}[-A(j\omega_{0^\circ})\,F(j\omega_{0^\circ})] = \text{Arg}[L(j\omega_{0^\circ})] = 0^\circ$

or $\text{Arg}[-A(j\omega_{0dB})\,F(j\omega_{0dB})] = \text{Arg}[L(j\omega_{0dB})] > 0^\circ$

where ω_{0dB} is defined as $|A(j\omega_{0dB})\,F(j\omega_{0dB})| = |L(j\omega_{0dB})| = 1$

Frequency and Phase Response (2/3)

- Bode Plots:
  - $|A(j\omega)\,F(j\omega)|$ & $\text{Arg}[-A(j\omega)\,F(j\omega)]$

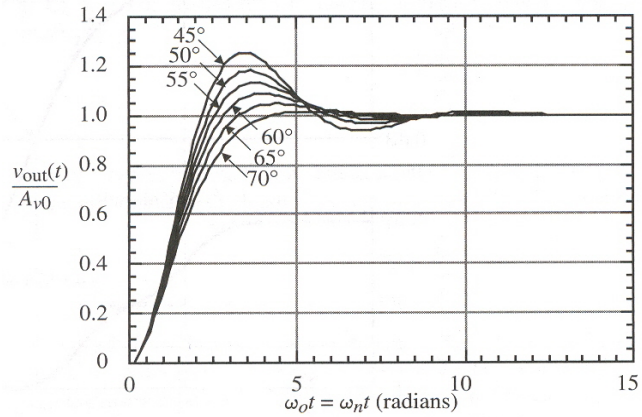


Phase Margin

$\Phi_M = \text{Arg}[L(j\omega_{0dB})]$

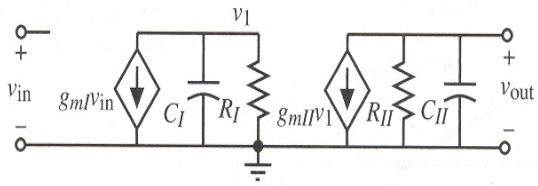
Frequency and Phase Response (3/3)

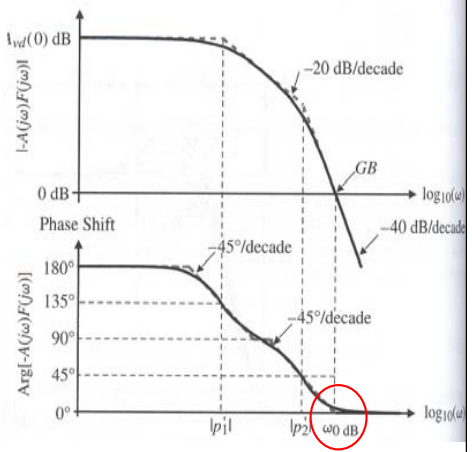
- Time response of a second-order system
  - Large P.M. results in less 'ringing' → good stability
  - P.M. >45° (at least), > 60° (preferable)



Second-order Uncompensated Op Amp

- Small-Signal Equivalent Circuit





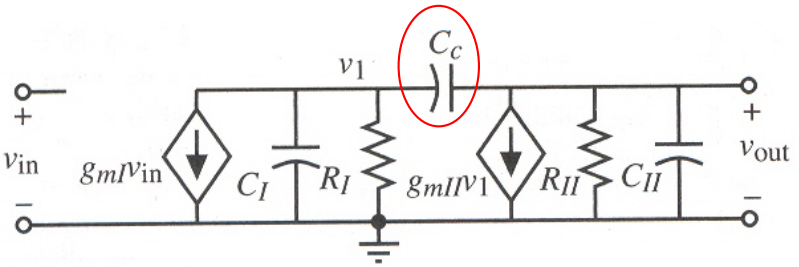
$P'_1 = -1/(R_I C_I)$

$P'_2 = -1/(R_{II} C_{II})$

If F(s)=1 (worst case)
PM << 45°
→need compensation

Miller Compensation of Op Amp

- Miller Compensation Technique



$P_1 = -1/(g_{mII} R_I R_{II} C_C)$

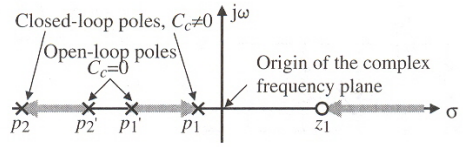
$P_2 = -g_{mII} C_C / (C_I C_{II} + C_C C_{II} + C_I C_C)$

$C_{II} >> C_I, C_C$ ↓ $\fallingdotseq -g_{mII}/C_{II}$

$Z_1 = g_{mII}/C_C$

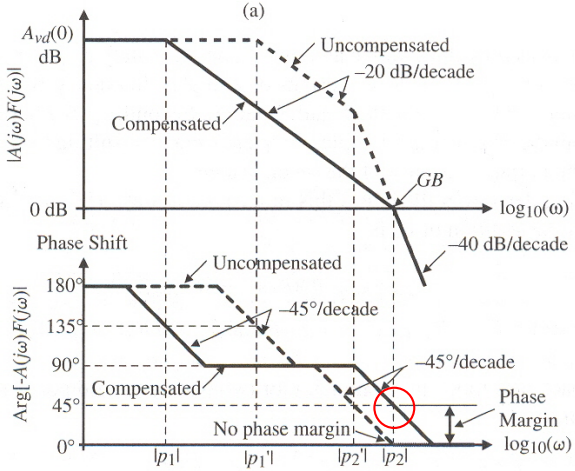
Miller Compensation of Op Amp

- Root locus plot of the loop gain F(s)=1



(a)

- Bode plots
  - P_2 does not affect the magnitude until after |AF|<1
  - Z_1 increases the phase shift



Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002

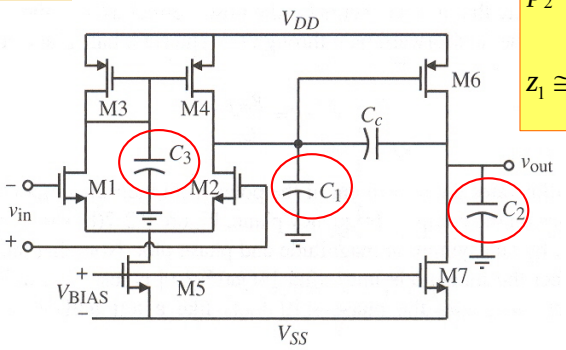
Two Stage Op Amp with Parasitic C

- There are more than two pole due to C_1, C_2, C_3,.....
- We will concentrate on two most dominant (small) pole and the RHP zero.

$$p_1 \cong \frac{-G_I G_{II}}{g_{mII} C_C} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6} C_C}$$

$$p_2 \cong \frac{-g_{mII}}{C_{II}} = \frac{-g_{m6}}{C_2}$$

$$z_1 \cong \frac{g_{mI}}{C_C} = \frac{g_{m2}}{C_C}$$



Unit gain bandwidth :

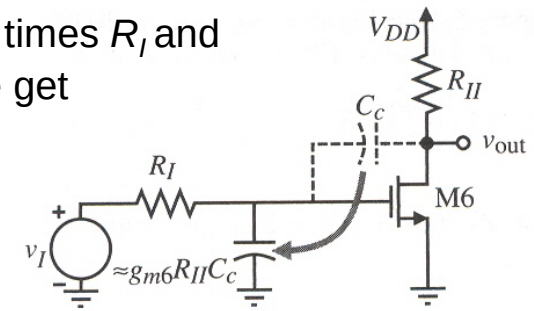
$$GB \cong \frac{g_{mI}}{C_C} = \frac{g_{m2}}{C_C}$$

Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002 u.edu.tw Page 122 / 195

Miller Compensation Technique

- **P_1 : *miller pole*** and accomplish the desire compensation
- M_6 is a NMOS. C_C is multiplied by the gain of the 2nd stage, $g_{mII}R_{II}$, to give a capacitor in parallel with R_I of $g_{mII}R_{II}C_C$
- Multiplying $g_{mII}R_{II}C_C$ times R_I and inverting it. Then we get

$$p_1 \cong \frac{-G_I G_{II}}{g_{mII} C_C} = \frac{-(g_{ds2}+g_{ds4})(g_{ds6}+g_{ds7})}{g_{m6} C_C}$$

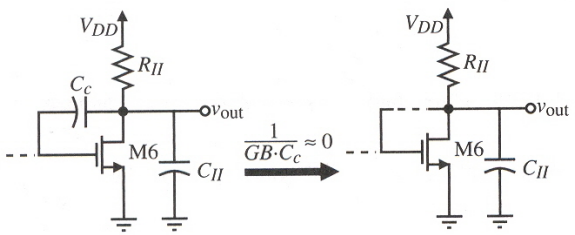


Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002 u.edu.tw Page 123 / 195

Miller Compensation Technique

- **P_2 : *output pole***, at least equal to GB and is due to the capacitance at the output of the op amp.
- C_{II} = C_L(load capacitance).
- Since $|p_2|$ is near or greater than *GB*, the reactance of C_C is approximately $1/(GBC_C)$ and is very small.
- M6 is a MOS diode and its small signal resistance is g_{m6}^{-1}.
- Multiplying g_{m6}^{-1}. by C_{II} and inverting gives

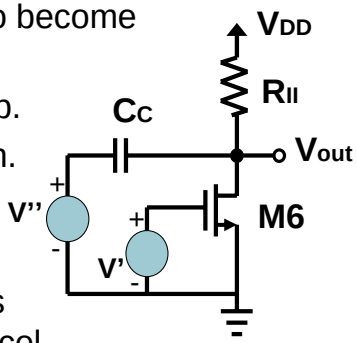
$$p_2 \cong \frac{-g_{mII}}{C_{II}} = \frac{-g_{m6}}{C_2}$$



Ref: P. E. Allen, D. R. Holberg, "CMOS Analog Circuit Design," 2nd Ed., Oxford, 2002 u.edu.tw Page 124 / 195

Miller Compensation Technique

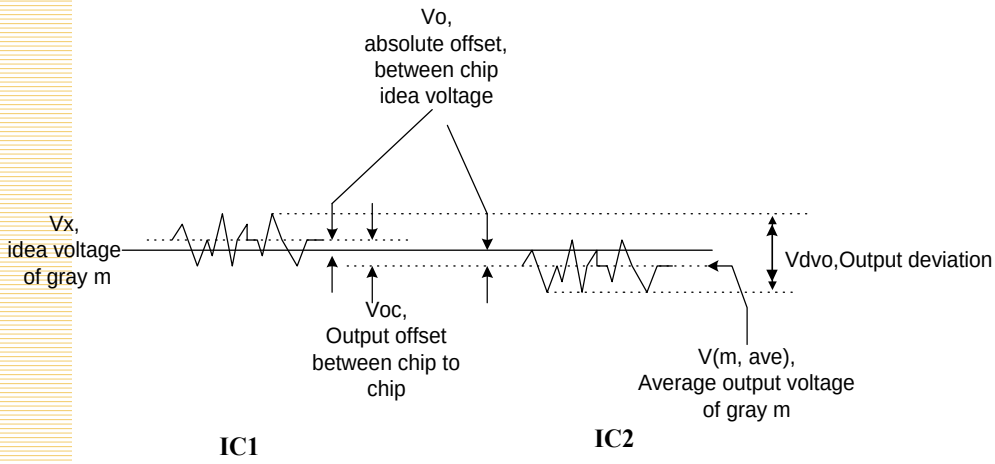
- Z_1 (the RHP zero) boosts the loop gain magnitude while causing the loop phase shift to become more negative. → *undesirable*
- It worsens the stability of the op amp.
- It comes from the two feedback path.



- The signals through these two paths may be equal and opposite and cancel, creating the zero.

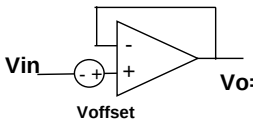
$$V_{out}(s)=\left(\frac{-g_{m6}R_{II}(1/sC_C)}{R_{II}+1/sC_C}\right)V'+\left(\frac{R_{II}}{R_{II}+1/sC_C}\right)V''=\frac{-R_{II}(g_{m6}/sC_C-1)}{R_{II}+1/sC_C}V$$

Output Deviation of Buffer

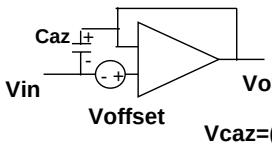


Offset Cancellation

Phase 1



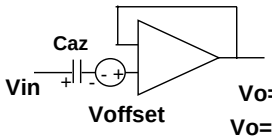
Vo=Vin+Voffset



Vo=Vin+Voffset

Vcaz=(Vin+Voffset)-Vin

Phase 2

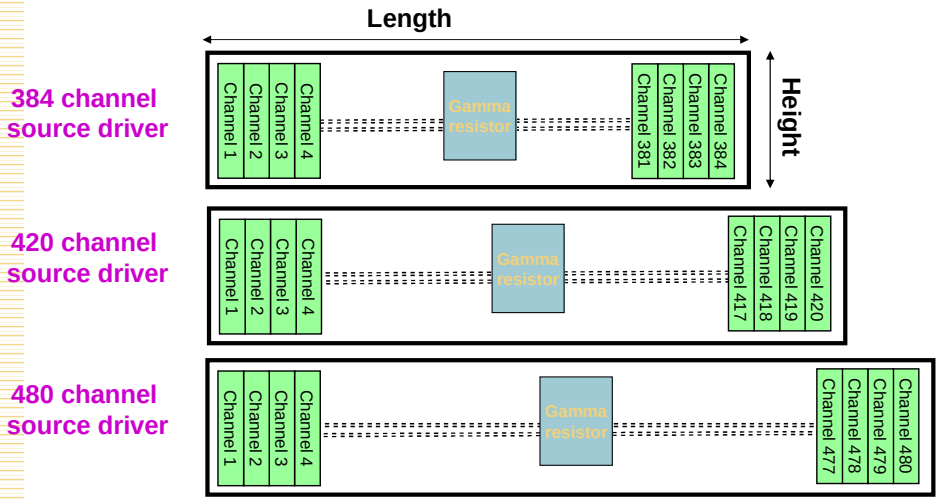


Vo=Vin+Voffset-Vcaz

Vo=Vin

◆How Long the Ph1 is enough to sample the correct Voffset?
◆How Long the Ph2 is enough to charge the pixel voltage?

Layout of Source Driver



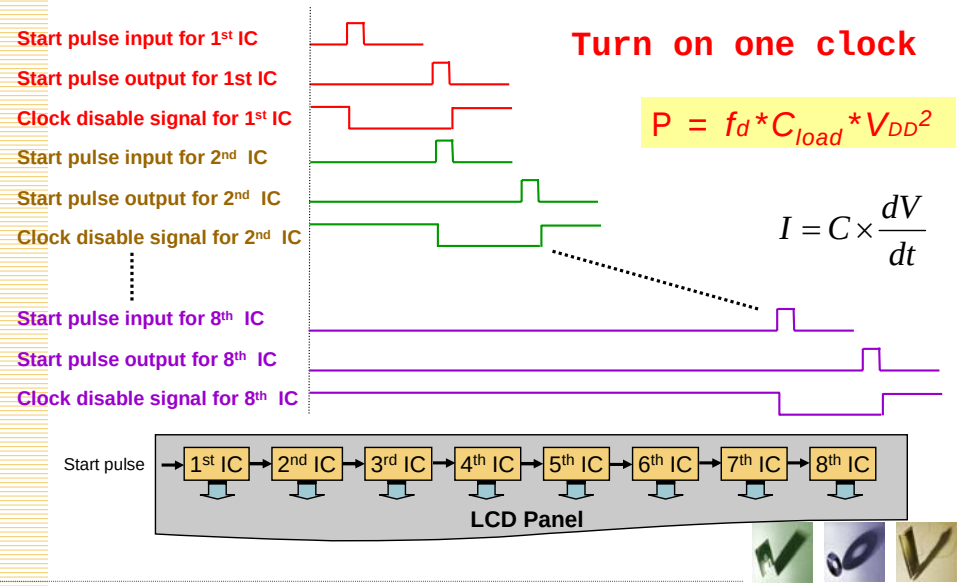
Layout length/channel ＜ 2 cm / 480 = 41 um

TSMC HV Process

High Voltage Process Characteristics

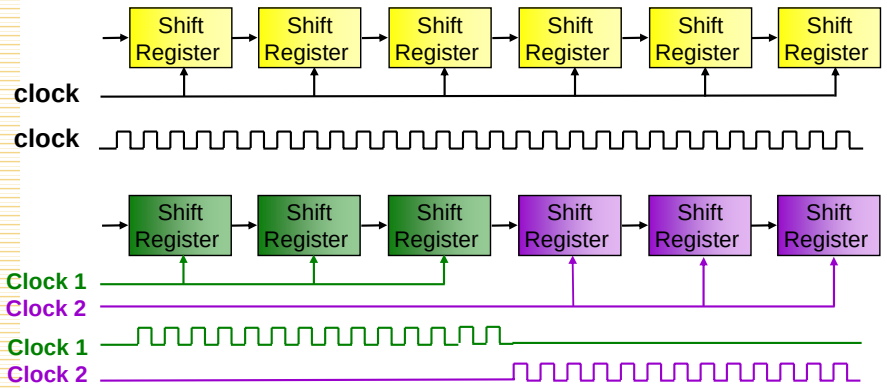
Technology	0.35-micron			0.25-micron	0.18-micron
	1-2P4M			1P5M	1P6M
HV / LV	12V / 3.3V	18V / 3.3V	40V / 3.3V	40V / 5V / 2.5V	40V / 5V / 1.8V
HV device structure	DDD	DDD	LDMOS	LDMOS	LDMOS
Well	Twin Well	Twin Well	Quad Well	Quad Well	Quad Well
Isolation	LOCOS			STI	
Capacitor type	PiP			MiM	
Idsat_N/P_HV (nA/μm)	400 / 250	260 / 170	400 / 230	400 / 230	400 / 230
Major Application	LCD Source Driver		LCD Gate Drive Power IC	One Chip Small Panel LCD Driver	
Process Ready	Yes	Yes	Yes	Yes	Yes
Logic Compatible	Yes				

Power Saving mode (1)



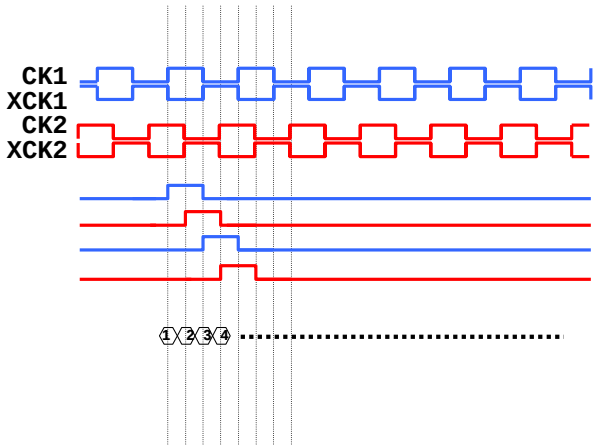
Power Saving mode (2)

Distribute clock tree

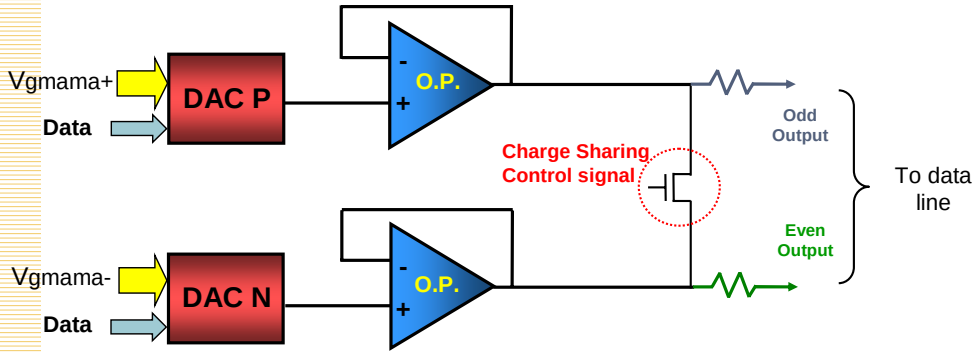


Power Saving mode (3)

Dual edge clocking

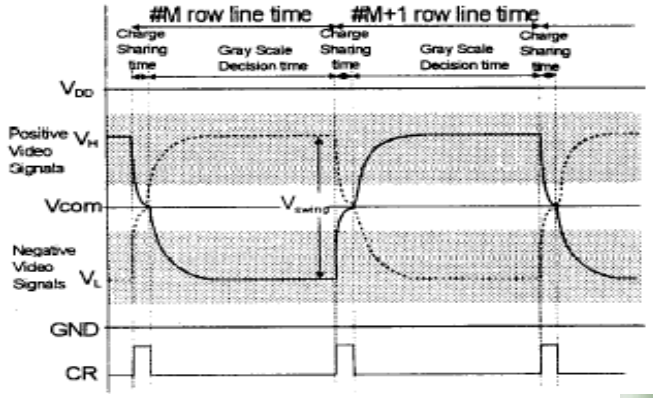


Charge Sharing

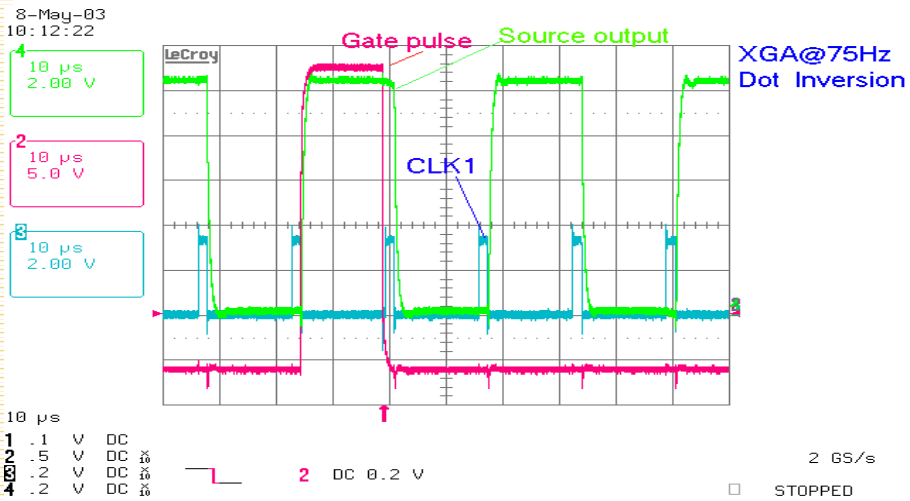


Charge Sharing

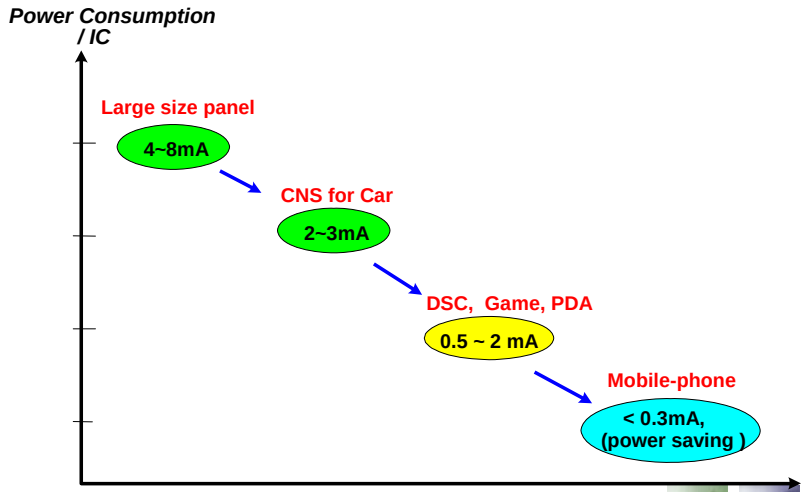
- **Because only half of the charges with positive potential are recycled, power saving efficiency of the previous charge sharing is theoretically limited to 50%.**



Waveform of LCD Driver



Power Consumption of LCD Source Driver



Trend of LCD Source Driver

- 6-bit / 8-bit to 10 bit resolution
- 384 / 480 to >500 output channels for SXGA+ / WSXGA+ / UXGA / WUXGA panel
- TTL to RSDS/mini-LVDS data interface for low power and EMI issue
- 10V to 18V for wide-view-angle panel
- Reduced chip size for cost down
- Low power consumption
- **TV application**

Outline

Ch4. Driving Circuits Design of A-Si TFT

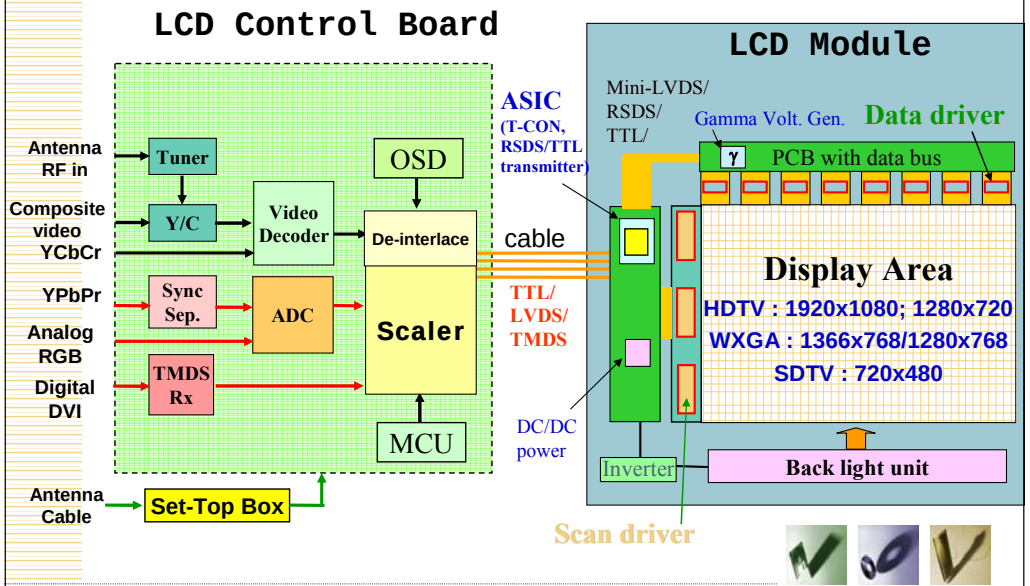
- **Gate Driving Circuit**
- **Source Driving Circuit**
- **LCD-TV Driving Technology**
- **Small-Size TFT-LCD Driver IC**
- **Trends of Digital Interface**

LCD TV vs. LCD Monitor

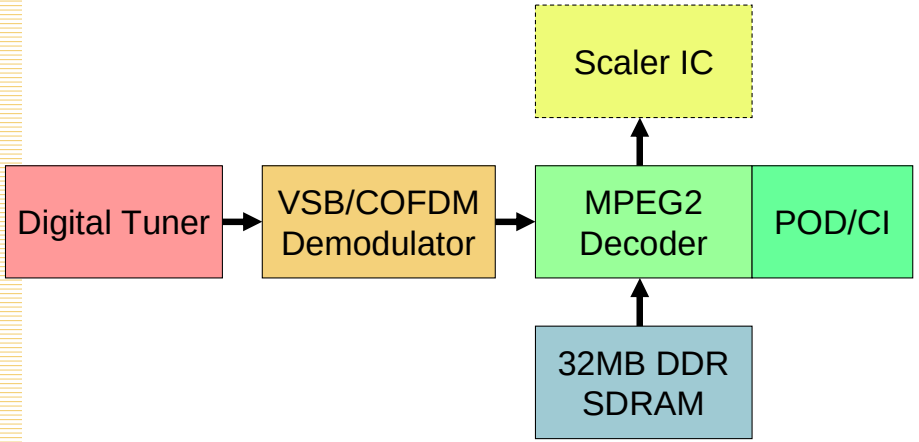
種類 / 性能	液晶顯示器	液晶電視
亮度	中亮度 (200~300 cd/m²)	高亮度 (400~500 cd/m²)
應答時間	8~16 ms	3~8 ms (採用OD液晶加速技術)
色域	72% NTSC色域 (i.e. sRGB規格)	90% NTSC色域
可視角度	120°(水平),90°(垂直)	170°(水平),170°(垂直)
觀賞對象	電腦資料與影片	電視映像,DVD映像

表1 液晶顯示器與液晶電視的性能比較

LCD TV Electronics

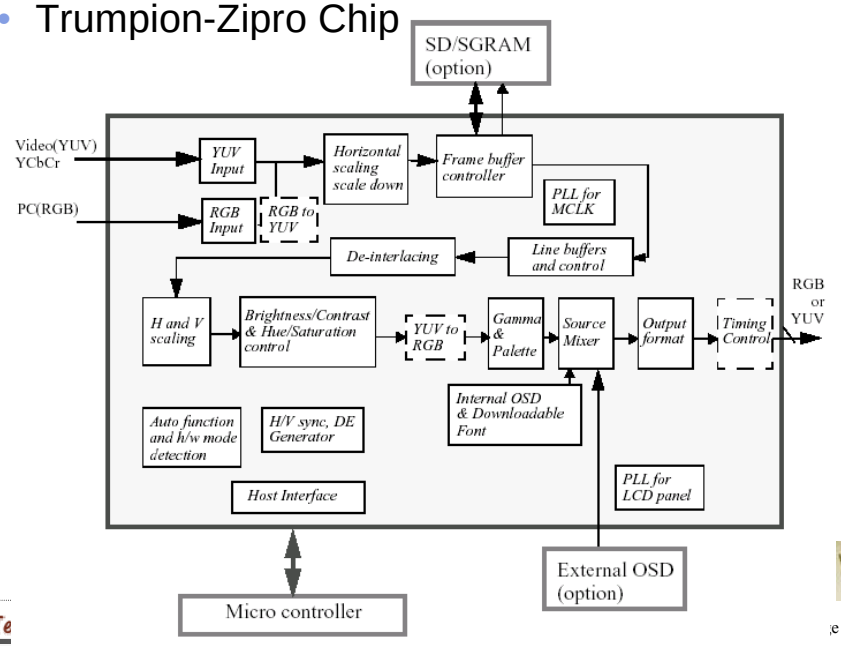


Digital TV System

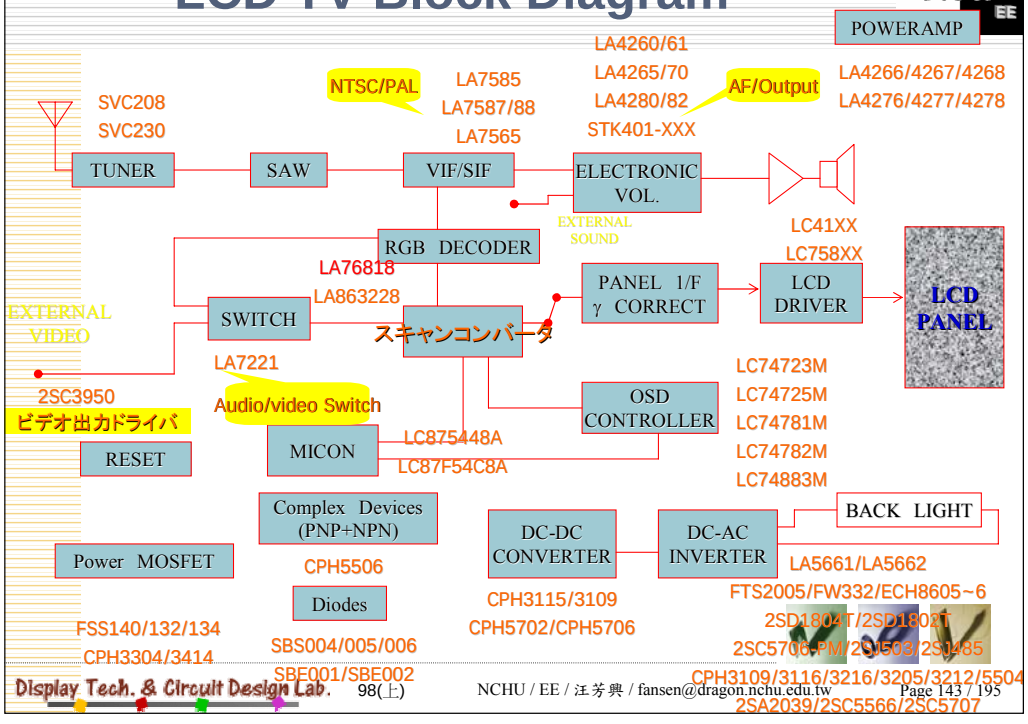


LCD-TV Control IC

- Trumpion-Zipro Chip

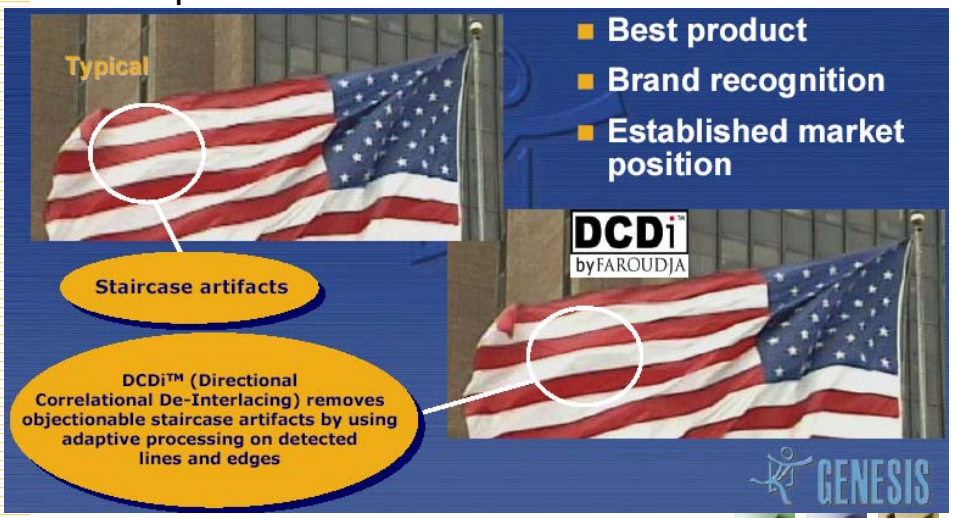


LCD TV Block Diagram

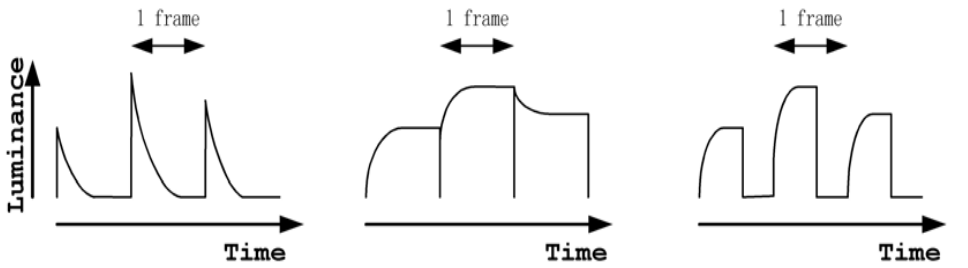


De-interlace

- example



Luminance of LCD vs. CRT

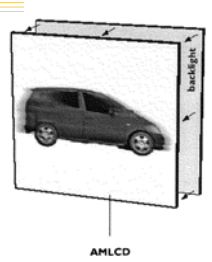


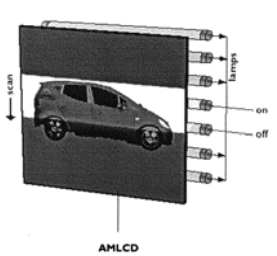
(a) CRT (Impulse Type) (b) LCD (Hold Type) (c) LCD (Impulse-like Type)

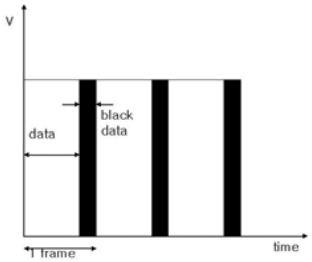
Display Quality for Moving Picture : Which is Better ?

Black Insertion

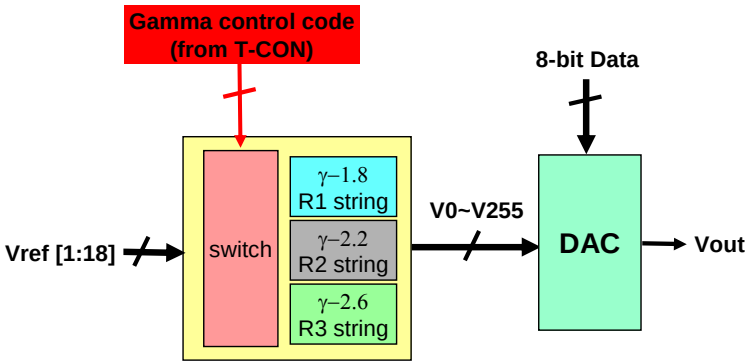
- Emulate impulse-type display
  - Turn off backlight
  - Insert black data or clear the data on pixel
    - **Double frame rate (60 -> 120 -> 240 Hz)**







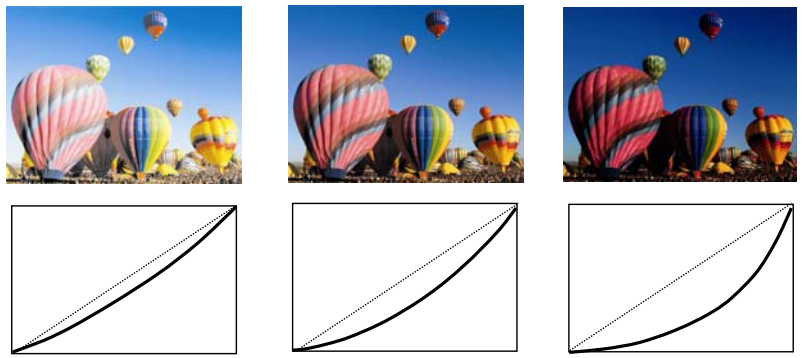
Adjustable Gamma Curve



Use external Gamma control code to control final Gamma resistance rings

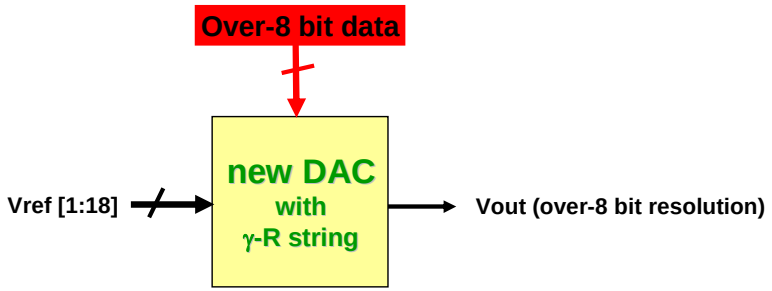
Adjustable Gamma Curve

example



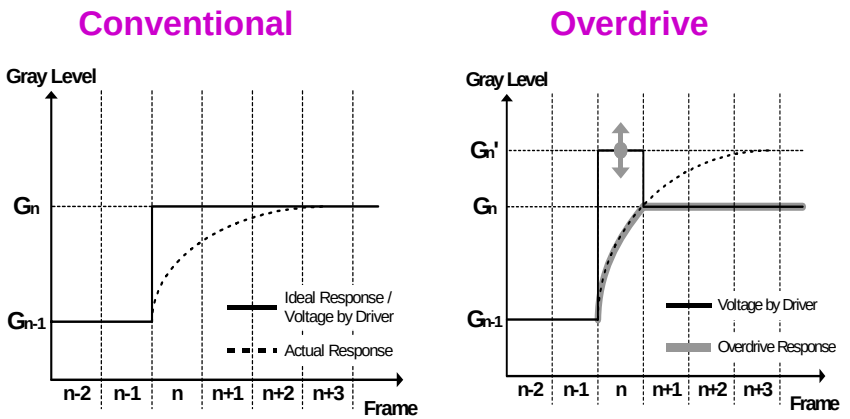
γ–1.8 γ–2.2 γ–2.6

Over 8-bit Color Depth



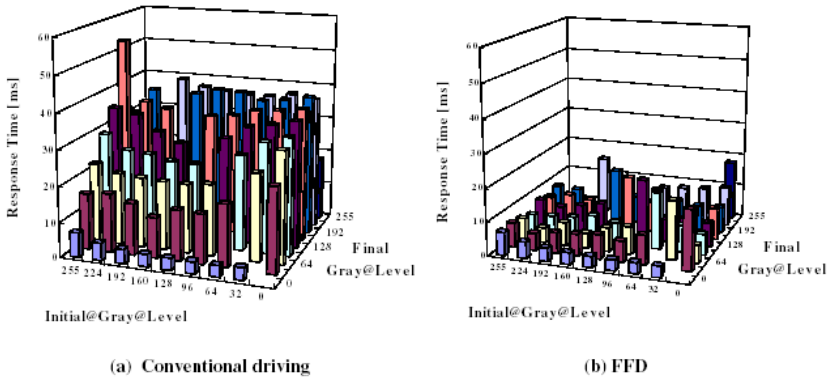
8 bit Source driver IC → 10 bit ! → 12 bit ?

Overdrive for LCD TV



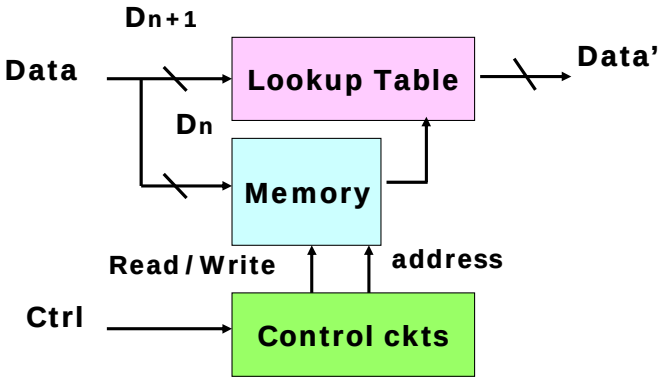
Effect on LC Overdrive

FFD (Feedforward Driving)Method by Mitsubishi



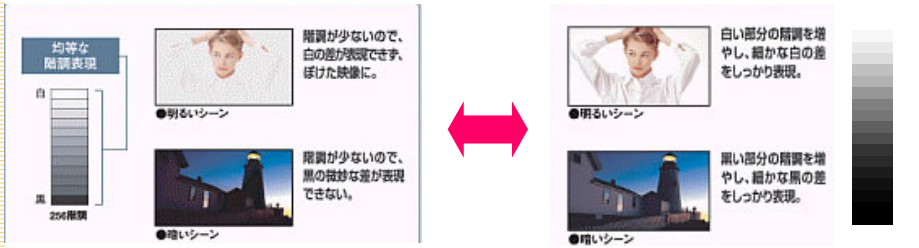
$T_r + T_f \approx 25ms$ (ON/OFF)
$T_r, T_f < 20ms$ (Gray Level)

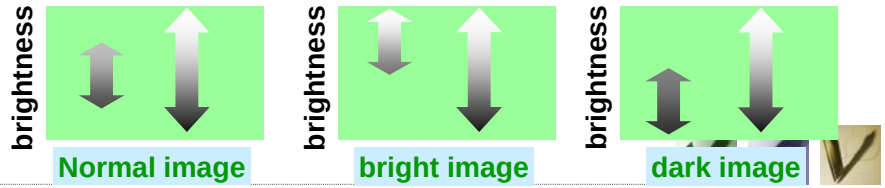
Overdrive Circuits



Dynamic Contrast Enhancement

- Over-8 bit color depth
- Dynamic gamma correction
- Dynamic backlight control



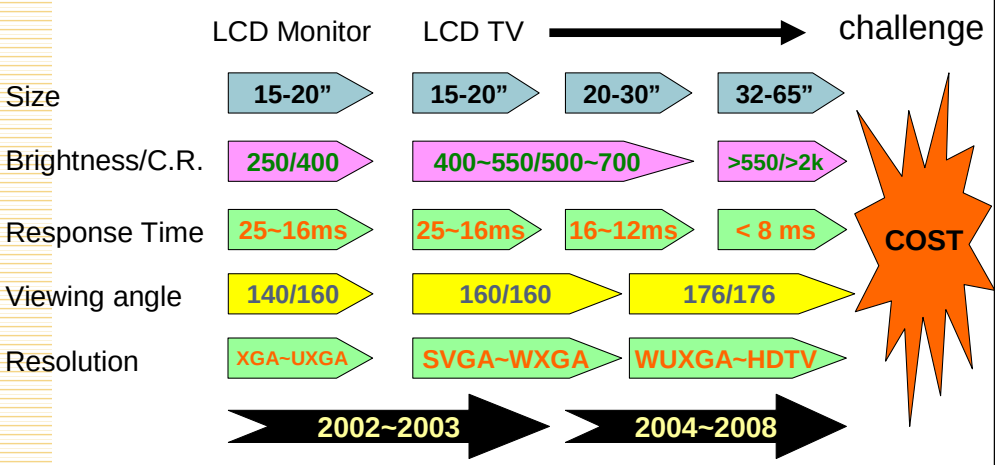


Other Technologies

- 10 bit color depth (source driver IC)
  - 1.07 billion colors
- LED backlight
  - R, G, B mixed LED BLU
    - **NTSC ratio > 100%**
    - **R/G/B color sequential method (CF-free)**
    - **Power consumption**
    - **Thin module thickness**
- Digital Image Processing
  - Sony:WEGA engine…

LCD TV Trends

Technology trends and challenges

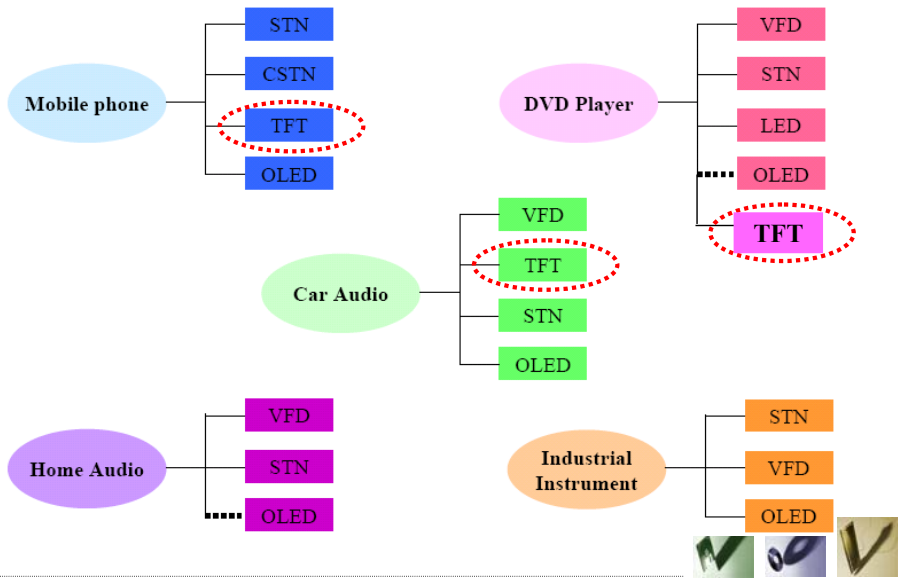


Outline

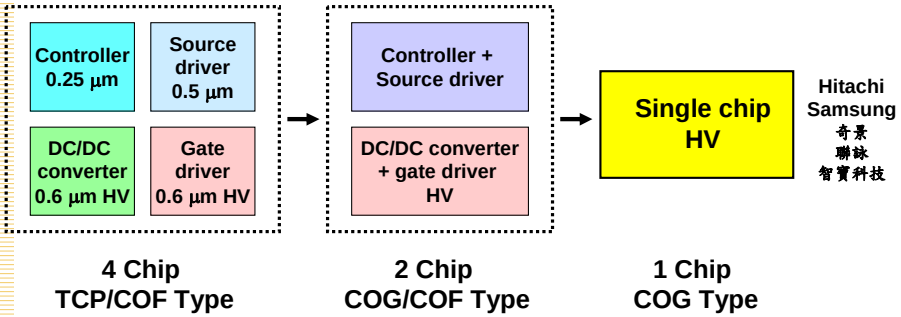
Ch4. Driving Circuits Design of A-Si TFT

- **Gate Driving Circuit**
- **Source Driving Circuit**
- **LCD-TV Driving Technology**
- **Small-Size TFT-LCD Driver IC**
- **Trends of Digital Interface**

Applications of Small Size Display



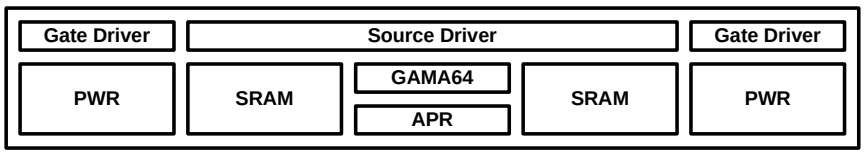
Small-Size TFT-LCD Driver IC



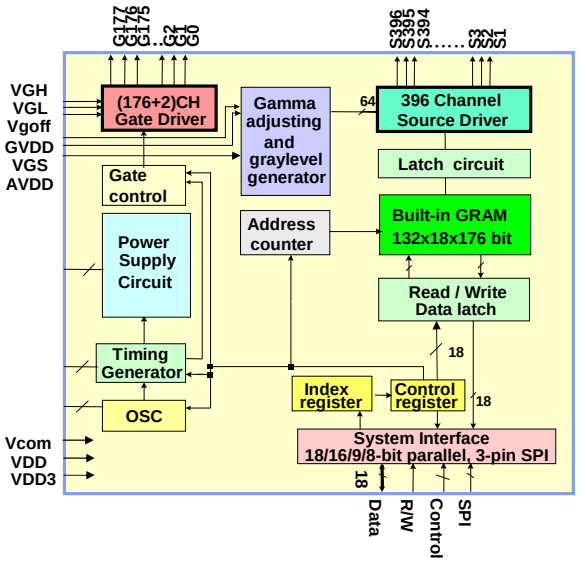
小尺寸TFT-LCD驅動晶片解決方案演進圖

Architecture of One Chip TFT-LCD Driver IC

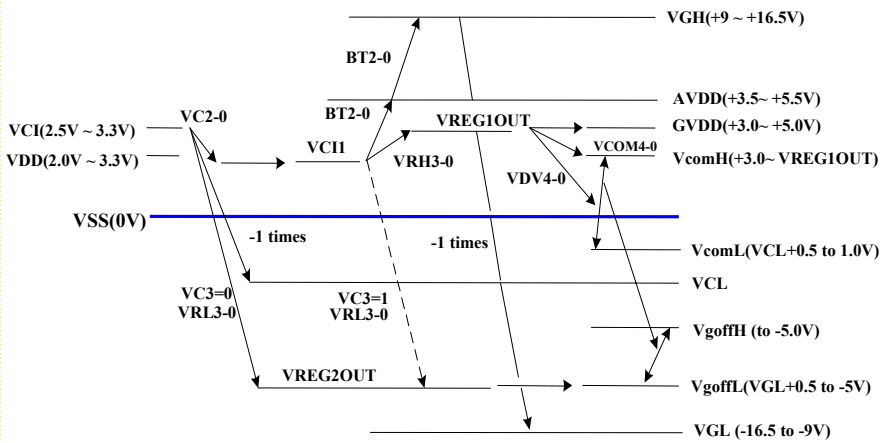
- Simple IC Sketch for TFT Mobile Phone
  - 2.5V Block：OSC, SRAM, APR, Some Logic
  - 5V Block：I/O, Source, Regulator, Charge Pump (PWR)
  - 32/40V Block：Gate, Regulator, Charge Pump (PWR)



Single Chip TFT-LCD Driver IC for Mobile Phone Application



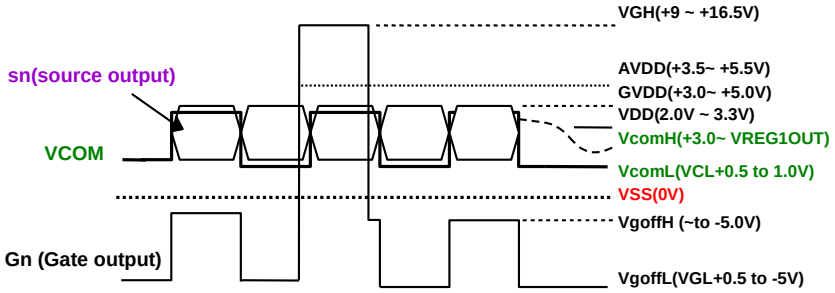
Voltage Setting



Note :

adjust the conditions of AVDD-GVDD > 0.5V, VcomL-VCL > 0.5V, and VgoffL-VGL > 0.5V with loads because They differ depending on the display load to be driven. In addition, Vci can be directly input to Vci1.

Voltage Waveforms



電壓波形設定示意圖

Power Pins Description (1/2)

Symbol	I/O	Description
VDD	-	System power supply. As NT3911 has internal regulator, VDD range varies with each mode. Non-regulated mode (PregB = 1) : +2.0 ~ +2.5 V Regulated mode (PregB = 0) : +2.0V
VDD3	-	System power supply for regulator as external power. (VDD3: +2.5 ~ +3.3 V)
AVDD	I/O	A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: +3.5 ~ +5.5 V) Connect this pin to VCI2 pin. When not using a charge-pump circuit 1, leave it open.
GVDD	I/O	Standard level for grayscale voltage generator. Connect a capacitor for stabilization.
VCI	I/O	An internal reference power supply for VREG1OUT/VREG2OUT. Connect VDD when VDD = 2.5 to 3.3 V. Connect a 2.5 to 3.3 V external-voltage power supply when VDD = 2.0 to 2.5 V.
VSS	-	System ground (0V)
AVSS	-	System ground level for analog circuit block.
VCL	I/O	A power supply pin for generating VcomL. When VcomL is higher than VSS, outputs VSS level.
REGP	I/O	Input pins for reference voltages of VREG1OUT when the internal reference-voltage generation circuit is not used. Leave these pins open when the internal reference-voltage generation circuit is used.
VREG1OUT	O	This pin outputs a reference voltage for VREG1 between AVDD and VSS. When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGP. Connect this pin to a capacitor for stabilization. When this pin is not used, leave it open.
VREG2OUT	O	This pin outputs a reference voltage for VREG2 between VSS and VGL When the internal reference voltage is not used, the reference voltage can be generated from the voltage of REGN. Connect this pin to a capacitor for stabilization. When this pin is not used, leave it open.
VcomOUT	O	A power supply for the TFT-display counter electrode. The alternating cycle can be set by the M pin. Connect this pin to the TFT-display counter electrode. This pin is also used as equalizing function: When EQ = "High" period, all source driver's outputs (S1 to S396) are short to Vcom level (Hi-z). In case of VcomL < 0V, equalizing function must not be used. (Set EQ bit (R07h) to be "00" for preventing the abnormal function.)

Power Pins Description (2/2)

Symbol	I/O	Description
VcomR	I	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between VREG1OUT and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	O	This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.
VcomL	O	When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
VGH	O	A positive power output pin for gate driver, internal charge-pump circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. Connect this pin to VCI3 pin. When not using a charge-pump circuit 2, leave it open.
VGL	O	A Negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. When internal VGL generator is not used, connect an external-voltage power supply higher than -15.0 V.
Vgoff	I	Power supply pin for off level for gate of TFT. Connect this pin to VgoffOUT. When VgoffOUT is not used, connect an external-voltage power supply higher than -TBD V.
VgoffOUT	O	An power output pin for gate driver. This pin is a negative voltage for the gate off level. Alternation can be synchronized by M pin. Set the internal register according to the structure of the TFT-display retention volume. For the amplitude at the alternation driving, this pin outputs a voltage between VcomH and VcomL with the VgoffL reference voltage..
VgoffH	O	When the Vgoff alternation is driven, this pin indicates a high level of Vgoff. Connect a capacitor for stabilization. When the CAD bit is low, the VgoffH output stops and a capacitor for stabilization is not needed.
VgoffL	O	When the Vgoff alternation is driven, this pin indicates a low level of Vgoff. Connect a capacitor for stabilization. An internal register can be used to adjust the voltage.

Power Definition (1/2)

(For the analog circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
LCD Supply Voltage	AVDD	3.5	-	5.5	V	For the analog circuit power
	VGH	9	-	16.5	V	
	VGL	-16.5	-	-9	V	
	VGOFF	-16	-	-5	V	
	GVDD	3	-	5	V	
Internal reference power supply voltage	VCI	2.5	-	3.3	V	
Output Voltage deviation	Vod	-	±20	-	mV	Source Driver
Output Offset between Chips	Voc	-	±20	-	mV	Source Driver
Dynamic Range of Output	Vdr	0.1	-	GVDD-0.1	V	S1 ~ S396
Source Driver Driving Current of Outputs	ISOH	50	-	-	uA	S1 ~ S396; Vo=4.5V v.s 3.5V AVDD=5V, Gradation output
Gate Driver Sinking Current of Outputs	IGOL	| -250 |	-	-	uA	G0 ~ G177; Vo=-12V v.s -11.5V VGH-VGOFF=30V
Gate Driver Driving Current of Outputs	IGOH	250	-	-	uA	G0 ~ G177; Vo=18V v.s 17.5V VGH-VGOFF=30V
Power consumption for Stand-by mode	Isc	-	-	5	uA	No load, VDD3=3V, VDD=2V, VCI=2.7V, VBS=VSS and all operating is stopped
Operating Current	IVDD	-	200	500	uA	
	IVCI	-	1.5	2.0	mA	

(VDD =2.0V, VDD3=3V, VSS =0V, TA=25 °C)

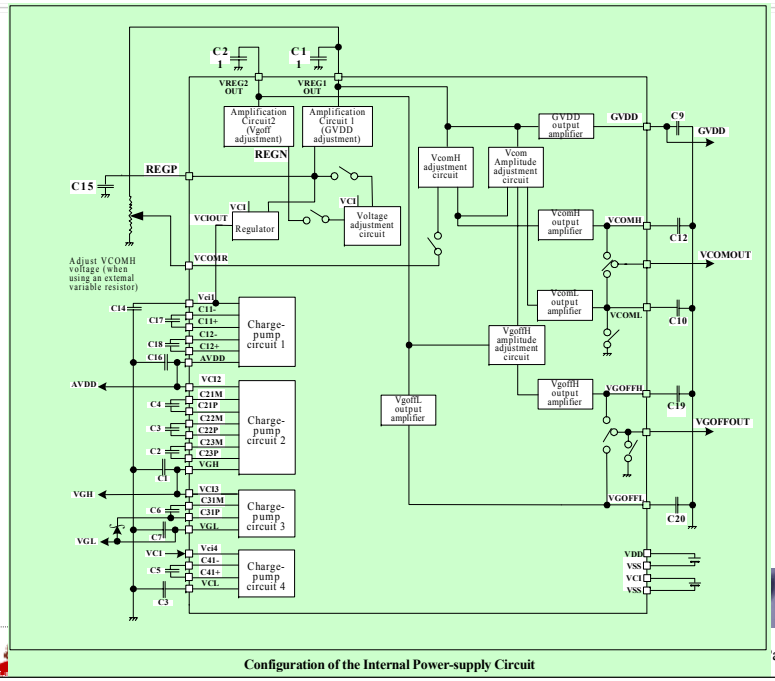
Power Definition(2/2)

(For the regulator circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reference voltage for internal digital power	RVDD	1.95	2.0	2.1	V	VDD3=3.3V
RVDD driving current	IRVDD	-	200	500	uA	
Reference voltage of VREG1OUT	REGP	2.46	2.5	2.56	V	VCI=3.3V, VC2-0="100"
Reference voltage for grayscale voltage generator	VREG1 OUT	5.71	5.83	5.95	V	VCI=3.3V, VC2-0="100", VRH3-0="1001"
VREG1OUT driving current	IVREG1	1	-	2.5	mA	
Reference voltage output for gate driver	VREG2 OUT	-6.47	-6.6	-6.73	V	VCI=3.3V, VRL3-0="0001"
VREG2OUT driving current	IVREG2	-500	-	-100	uA	
GVDD driving current	IGVDD	100	-	150	uA	
High level reference voltage of Vgoff	VgoffH	-0.85	-0.83	-0.81	V	VCI=3.3V, VC2-0="100", VRH3-0="1001", VDV4-0="01101"
Low level reference voltage of Vgoff	VgoffL	-6.47	-6.6	-6.73	V	VCI=3.3V, VRL3-0="0001"
High level reference voltage of Vcom	VCOMH	4.57	4.66	4.75	V	VCI=3.3V, VC2-0="100", VRH3-0="1001", VCM4-0="10101"
Low level reference voltage of Vcom	VCOML	-1.13	-1.11	-1.09	V	VCI=3.3V, VC2-0="100", VRH3-0="1001", VDV4-0="01101"

(Reference for system design)

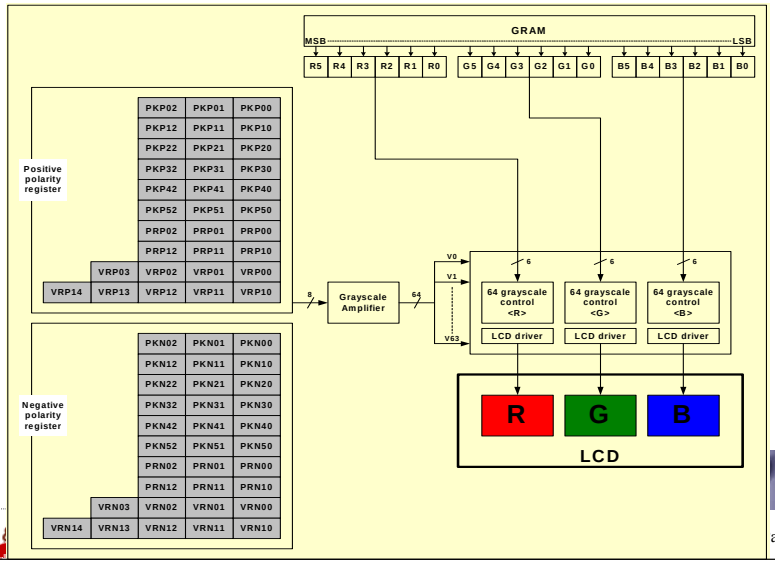
Power Supply Circuits



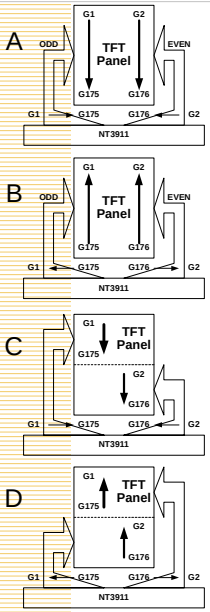
Configuration of the Internal Power-supply Circuit

GAMMA ADJUSTMENT FUNCTION

- The NT3911 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels.



Scan Mode

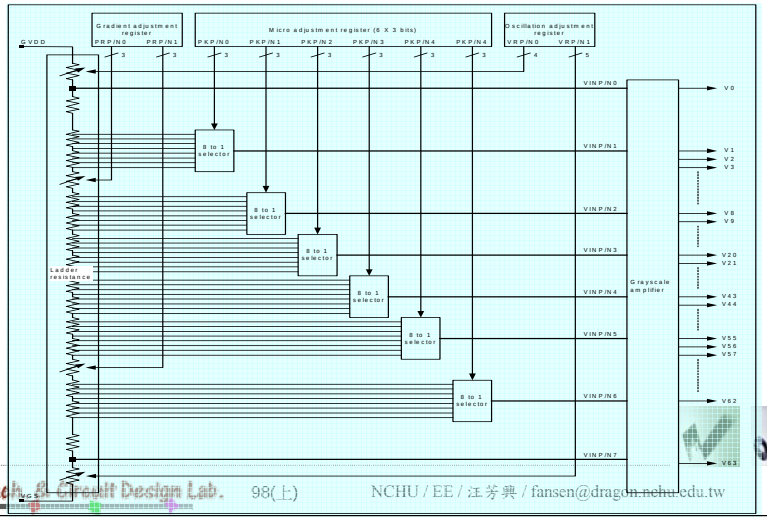


• Gate scan mode of NT3911 is set by SM and GS bit. GS bit determines the scan direction whether the gate driver scans forward or reverse direction. SM bit determines the method of display division (Even/Odd or Upper/Lower division drive). Using this function, various connections between NT3911 and the liquid crystal panels can be accomplished

SM	GS	Scan Mode	
0	0	A	G1→G2→G3→G4→…→G173→G174→G175→G176
0	1	B	G176→G175→G174→G173→…→G4→G3→G2→G1
1	0	C	G1→G3→G5→…→G173→G175 →G2→G4→G6→…→G174→G176
1	1	D	G176→G174→G172→…→G4→G2 →G175→G173→G171→…→G3→G1

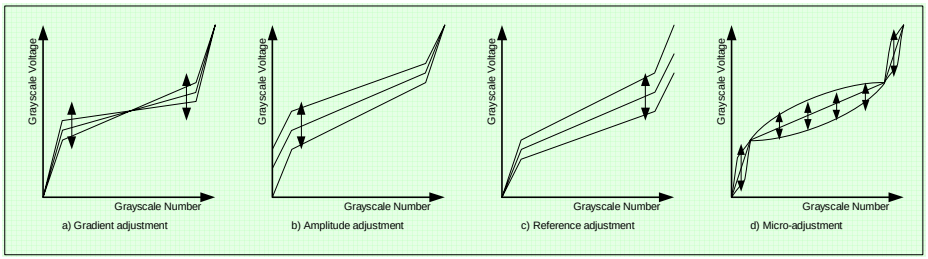
Structure of Grayscale Amplifier

• The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Each level is split by the internal ladder resistance and level between V0 to V63 is generated.



Gamma Adjustment Register

• This block has the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4-type of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (average <R><G><B> are common.) The following figure indicates the operation of each adjusting register.



Chip Size & Pad Dimensions

Items	Pad name.	Size		Unit
		X	Y	
Chip size	-	20720	2500	um
Pad size	Input Pad	54	100	
	Output Pad	36	70	
	Dummy Pad 1,195,239,742	80	80	

• **NOTES:**
• Scribe line included in this chip size (Scribe line: 120um)

Process Feature for One Chip Driver IC

Technology	0.25um 1P3M (MIM Process)
LV (Dual Gate) / HV	2.5V / 5V / 40V (+/-20V)
Oxide Thickness	48A / 110A / 1000A
40V HVMOS Structure	LDMOS
LV / HV Well Structure	Retrograde / Drive-In Well + NBL
Isolation	STI / P-EPI
Gate Material	Poly (S/D Implant Doped) + Salicide
S / D Area	Salicide
Capacitor	MIM
High Rs Poly	400~2000 Ohm

Source : Novatek training material

Product Applications

- TFT Driver IC for Mobile Phone

Amorphous-Silicon TFT Mobile Phone Driver IC Product Line				
	NT3911	NT3912	NT391X	NT391X
Panel Category	Single	Single	Single	Dual
Display Size	132*176	176*240	X	X
Display Color	262k	262k	262k	262k
SRAM Size	418k	760k	X	X

- STN Driver IC for Mobile Phone
  - NT7523爲Hi-Fas CSTN One Chip Driver IC，使用0.25μm 2.5/5/32V Process

Source : Novatek training material

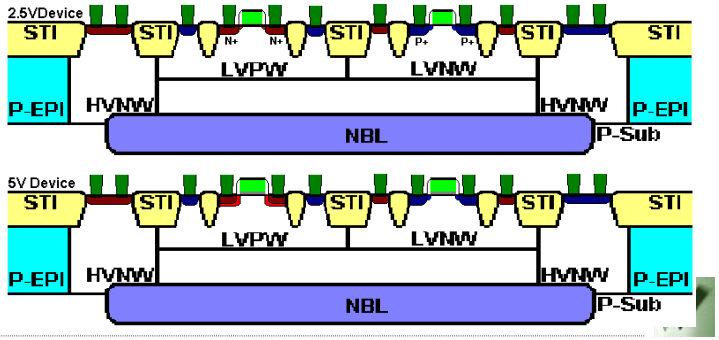
LV and HV Device Type

● LV and HV Device Type and Related Data (1)

✹ 2.5 / 5V Devices Characterization

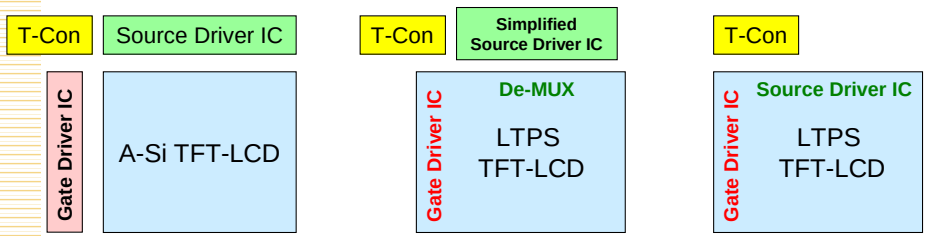
- 5 LV Devices (2.5V NMOS and PMOS, 5V NMOS and PMOS, 2.5V Native NMOS)
- STI Field Isolation
- Triple Well Structure
- Salicide Structure

✹2.5 / 5V Devices Cross Section Sketch



Source : Novatek training material

LTPS TFT-LCD Driver ICs



Conventional a-Si TFT-LCD

LTPS TFT-LCD Example 1

LTPS TFT-LCD Example 2

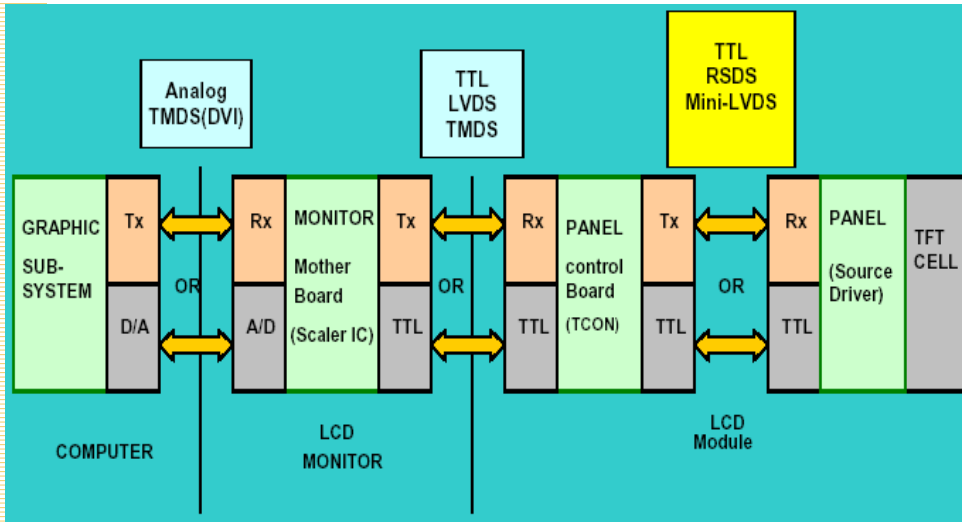
非晶矽與多晶矽 TFT-LCD 驅動方式比較圖

Outline

Ch4. Driving Circuits Design of A-Si TFT

- Gate Driving Circuit
- Source Driving Circuit
- LCD-TV Driving Technology
- Small-Size TFT-LCD Driver IC
- Trends of Digital Interface

Interfaces in TFT-LCD Monitor



Digital vs. Analog

	TMDS	Analog RGB
signal	Digital	Analog
Tx distance	>5M	<2M
Image quality	•Good •Differential pair •Low swing	•Bad •Depend on cable and noise •Depend on ADC
other	•TMDS Tx in Graphic card is needed •TMDS Rx in scaler is needed	•DAC in Graphic card is needed •ADC in scaler is needed

Panel Input Interface

	resolution	Interface	1/2 port	Freq.
NB	XGA	LVDS	1	65MHZ
	SXGA,SXGA+	LVDS	2	54MHZ
Monitor	XGA	TTL	2	32.5MHZ
		LVDS	1	65MHZ
	SXGA,SXGA+	LVDS	2	54MHZ
		TTL	2	54MHZ
	UXGA	LVDS	2	81MHZ

TTL vs. LVDS

	TTL	LVDS
Pin count	•60~80pin Connector •large PCB area and data bus	•20~30pin Connector • small PCB area and data bus
Cost	•cheap •PCB large •Extra R,C,bead in input data	• expensive(Tx,Rx) •PCB small •Extra R,C,bead in input data is not needed
Signal quality	Bad→Data coupling	Good→differential pair
Distance	Short	Longer
Frequency	Operation in low frequency	Can operation in high frequency
EMI	Bad •3.3V •Extra R,C,Bead is needed for reduce EMI	Good • Vcom=1.2V,swing=350mV •PCB layout skill need concern more • terminal resistor is need
Power consumption(bus)	High(3.3V)	low
Application	Monitor	NB/Monitor

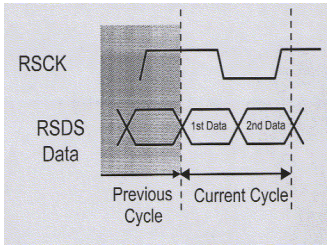
Comparison of TTL，RSDS，and Mini-LVDS

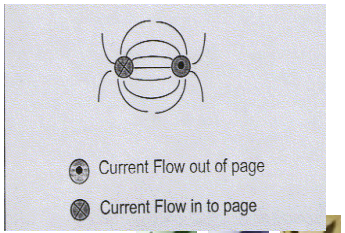
		TTL	RSDS	Mini-LVDS	Remark
Bus lines	8-bit	24X2	24	12	
	6-bit	18X2	18	10	
Voltage Swing		3.3V	200mV	200mV	Lower amplitude for reducing EMI
Frequency	XGA	32.5M (2 ports)	67M (1 port)	67M (2 ports)	
	SXGA	54M (2 ports)	54M (2 ports)	108M (2 ports)	
	UXGA	-	81M	162M	
LCD Application		~SXGA	~ UXGA	~ QXGA	
PCB Area		1	0.7~0.8	0.5~0.7	
T-CON Pins	6-bit	~100	~64	~100	
Driver IC Input Pins	6-bit	~80	~60	~50	

Remark: RSDS and Mini-LVDS use twin-pair lines

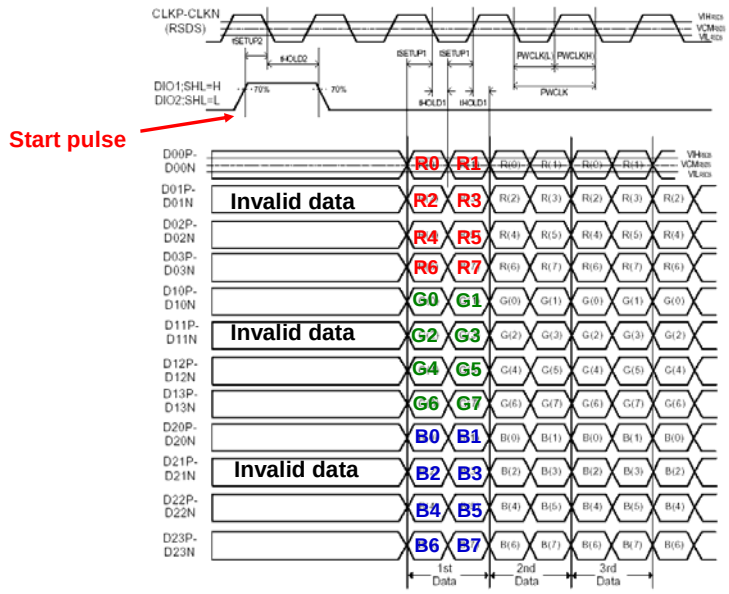
RSDS Definition

- Reduced Swing Differential Signal
  - ±200 mV swing (typical)
  - 2:1 mux - 2 data per clock cycle
  - 100 ohm differential terminals
  - Voffset = 1.2 V
  - RGB data and clock only
- Apply to bus between T-Con and source drivers
  - Reduce EMI
  - Reduce power consumption
  - Reduce source driver bus width



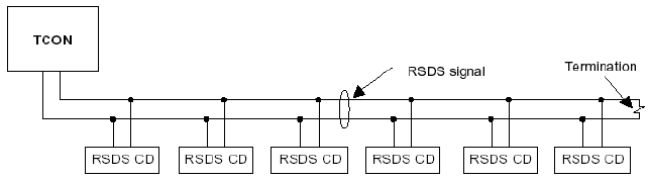


8 Bit RGB RSDS Data

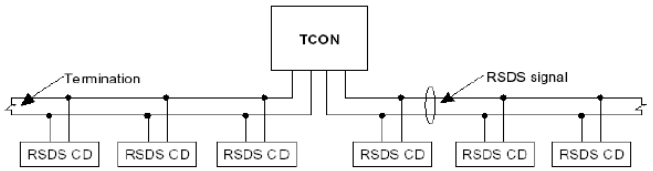


System Diagram ： RSDS Configuration

Single-end



Front / Back

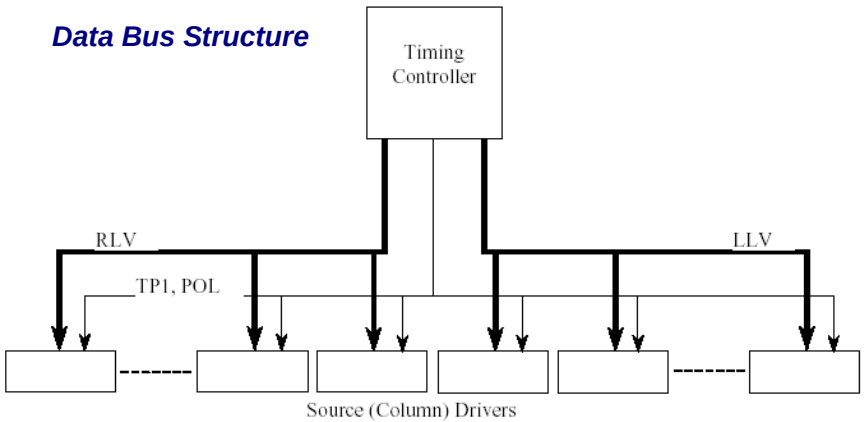


RSDS Features and Benefits

- Reduced pin T-Con counts
  - Enable smaller area PCBs
- Reduced number of components
  - Small area PCBs
  - Lower cost
  - Number of components：TTL:RSDS = 190:101 (in 14.1" XGA) → 46.8% reduction
- Reduced number of PCB layers
  - Number of layers：TTL :RSDS = 6:4

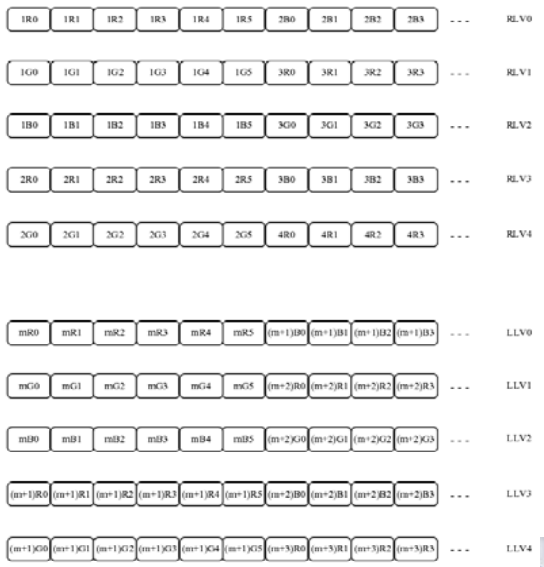
Mini-LVDS

Data Bus Structure



Mini-LVDS

6 bit data, 5 pairs



Mini-LVDS

8 bit data,

6 pairs

RSDS vs. Mini-LVDS

	RSDS	Mini-LVDS
PCB Size	Larger	Smaller
TCON	XGA: TQFP64/80 SXGA/UXGA:TQFP128/144	TQFP100
Driver Size	Same	Same
Frequency Limitation	DIO(Start Pulse)	No
Resolution Limitation	<= UXGA/Dual Buses	QXGA or larger/Dual Buses
Possible Driver Vendors	More	Limited

- ***RSDS is the major interface***
- ***Mini-LVDS become important for high resolution panel***

Point to Point Differential Signaling (PPDS)

- PPDS is based largely on the RSDS™
- Advantages:
  - The total number of input signals for each column driver is greatly reduced.
    - 8-bit RSDS system: 12 data pairs and the clock pair by each column driver.
    - In a PPDS system: signal data pair and a clock pair
    - 26 in RSDS ➔ 4 in PPDS

Parameter	RSDS	PPDS
Differential Signal Level	±200mV	±200mV
Common Mode Voltage	1.3V	0.8V
Typical Output Current	2mA	2mA
Transmission Lines	50Ω	50Ω

Table 1. Comparison of PPDS and RSDS levels

PPDS™

- Advantages: (cont.)
  - improved signal integrity.
    - typical RSDS bus architecture
    - ➔ vias and stubs on every signal line ➔ creates a large number of impedance discontinuities.
    - point to point system➔ no vias and stubs➔ data signal maintain higher level➔ Higher color depth
  - Major improvement in EMI
    - Due to the incoming LVDS clock and PPDS clock operating at different frequency.

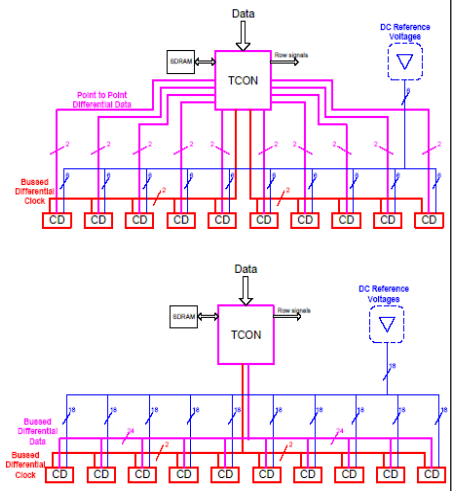


Figure 1. Typical 8-bit panel configurations for PPDS (top) and RSDS (bottom)

PPDS Protocol

- The total reduction in data signals from an RSDS based system to the PPDS architecture.
- The protocol is split into 5 required interval and 1 optional interval.

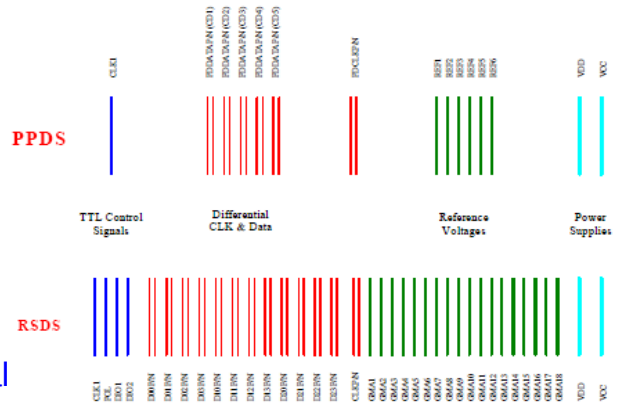


Figure 3. Total number of traces for the PPDS interface compared to RSDS

Summaries

Technology Trends of Large-Size TFT-LCD Source Driver IC

LCD高精細化	XGA (1024x768)	SXGA (1280x1024)	UXGA (1600x1200)	WUXGA/HDTV (1920x1200)
LCD多色階化	6-bit (64灰階)	8-bit (256灰階)	10-bit (1024灰階)	
LCD廣視角化	TN+Film (R60/L60/U60/D40) 8~10V	MVA/IPS (R80/L80/U80/D80) 12~17V	OCB	
LCD多Pin化	300~384 pin Pitch 50~70um	384/480 pin Pitch 30~50um	480 pin	>500 pin
LC快速反應	>25ms	16ms	12ms	8ms 3ms Overdrive→
LCD狹緣幅化	TCP	COG	COF	
Data高速化	50~70 MHz	60~85 MHz		

Memo