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BOK—Underfill Optimization for FPGA Package/Assembly

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Objectives and Products

Commercial-off-the-shelf area array package (COTS AAP) technologies in high-reliability versions are now being considered for use in a number of National Aeronautics and Space Administration (NASA) electronic systems. Although a number of these advanced electronic packages commonly use underfill within the package, including under the flip-chip (FC) die; full or partial corner underfilling may also be required at the printed circuit board (PCB) level to improve assembly reliability, particularly under mechanical and fatigue loading. There is extremely limited test-verified guideline for use of underfill for NASA with the stringent requirements on materials and reliability. In preparation for developing a test matrix and implementation, a survey of literature and current practices and reliability issues are carried out.

This report presents a summary of literature surveyed and provides a body of knowledge (BOK) gathered on the characterization methods for underfill materials. It first discusses the key characteristics of polymeric adhesives, since underfill is an adhesive specially modified to fill the gap (underfill) between adherents. Then, the report presents the thermal cycle reliability of underfill for flip-chip die with conventional balls, which is a well matured and recent advanced version with fine copper-pillar interconnects. In addition, it provides a brief discussion on the more common process of underfilling, including capillary and snap cure, and then touches on the types of residual stresses induced on adherents and solder interconnection due to the underfill cure process.

The report emphasizes reliability due to underfilling at the board level, discussing key parameters that influence thermal cycle and mechanical reliability of underfill, edge-bond, and corner stake in detail, referencing surveyed literature and a few recently presented conference papers. In particular, reliability information was gathered for fine pitch ball grid array (FPBGA) and ceramic BGA assemblies. Understanding key characteristics of underfill materials, as well as the process and quality assurance (QA) indicators for reliability, are important in judicially selecting and narrowing the follow-up applicable test methods in preparation for low-risk insertion of the advanced electronic packages.

Key Words: Underfill, solder joint reliability, thermal cycle, mechanical fatigue, drop, FCBGA, CGA, CSP, FPGA, flip chip ball grid array, flip-chip column grid array

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1. Executive Summary

Polymeric adhesives have been used extensively at the package and assembly levels for high reliability microelectronics applications. Indeed, NASA generated the first specification on adhesives—controlling ionic, outgas, and volatile levels—for use in space applications. However, this is not the case for the use of underfill in advanced electronics single and stack packaging technologies, where commercial industry is the leader. Underfill is a specially formulated polymeric adhesive that fills the gap between the die/package and substrate/PCB (printed circuit board) and relieves stresses on fragile solder interconnections. Investigation of underfill behavior becomes extremely important with the recent emergence of advanced field programmable gate arrays (FPGA) and their use in high-reliability applications. There are currently two versions of high input/output (I/O) microelectronic devices: the non-hermetic underfilled flip-chip ball grid array (FCBGA) and the flip-chip column grid array (CGA). A class Y is being assigned to cover the category of non-hermetic CGA packages.

For the advanced packages, use of underfill under the die is a must at the package level and may or may not be required at the assembly level, i.e., when these packages are assembled onto PCB. For flip-chip die, underfill is applied to fully cover the area under the die, whereas for package assembly, full or partial (such as an edge or corner) coverage may be considered. Use of edge bonding is investigated for commercial use; corner staking is a common method for high-reliability applications. Figure 1 schematically illustrates use of underfill, at both the package and assembly levels.

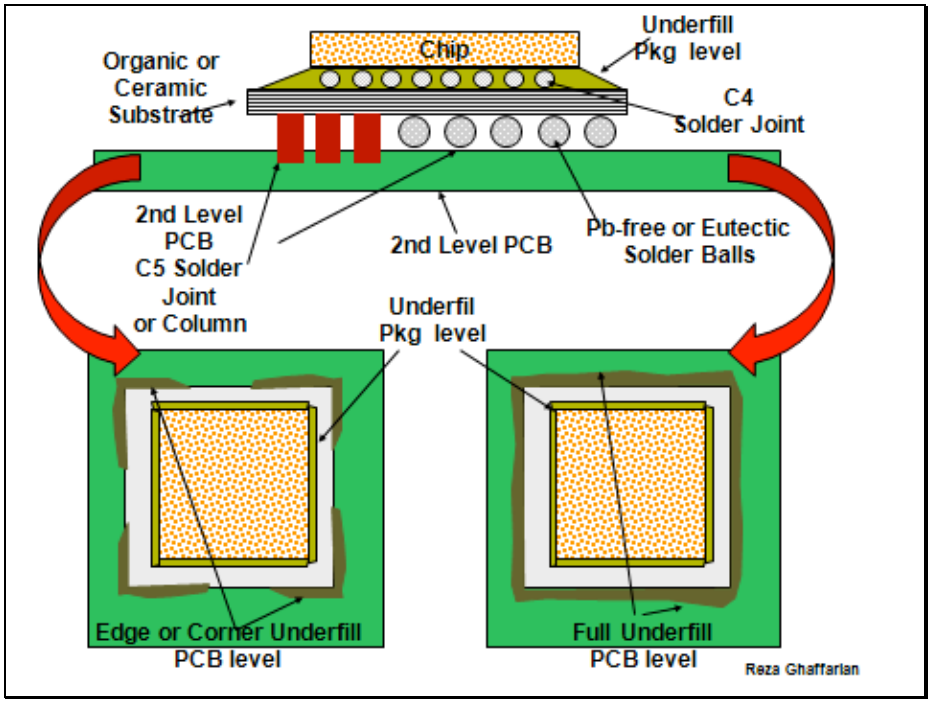

Figure 1. Underfill application at the package level under the flip-chip die and at the assembly level for high I/O flip-chip ball/column grid-array (FCBGA) packages.

At the package level, use of exposed underfill causes classification changes to non-hermetic devices, with additional testing requirements for high-reliability application. Significant efforts by package suppliers and users are being carried out to better understand the limitations of these types of non-hermetic packages. Indeed, a new specification is being generated for class Y non-hermetic packages with additional specific qualification testing required to narrow their use with underfilled flip-chip die. Underfill-specific material requirements for high reliability and space-relevant requirements are being addressed, such as the inability to verify the integrity of individual solder balls (commonly verified by pull testing for wire bond attachment) and outgassing and ionized radiation.

This report provides a survey of the available literature on the characterization methods for underfill materials. It discusses the key characteristics of polymeric adhesives, including thermoplastic and thermoset. Underfill is a specially formulated adhesive that fills the gap between die/package and substrate/PCB with easy processing and improves the thermal and mechanical integrity of devices/packages. Conventional underfill uses the capillary behavior of resin, whereas other underfills (e.g., snap cure) are developed to improve processing throughputs. Stresses are induced after curing due to CTE mismatch of underfill and adherents. A simple calculation for residual stress level is provided. For flip-chip die, underfill significantly improves thermal cycle resistance. Experimental data are presented that show improvement in reliability for underfilled flip-chip die compared to those with no-underfill conditions. Data are presented for both die with conventional balls and those recently introduced with much finer copper pillar interconnects. Figure 2 schematically shows the level of improvement in thermal cycles to failure for flip-chip die, which depend on a variety of adhesive and adherents material characteristics.

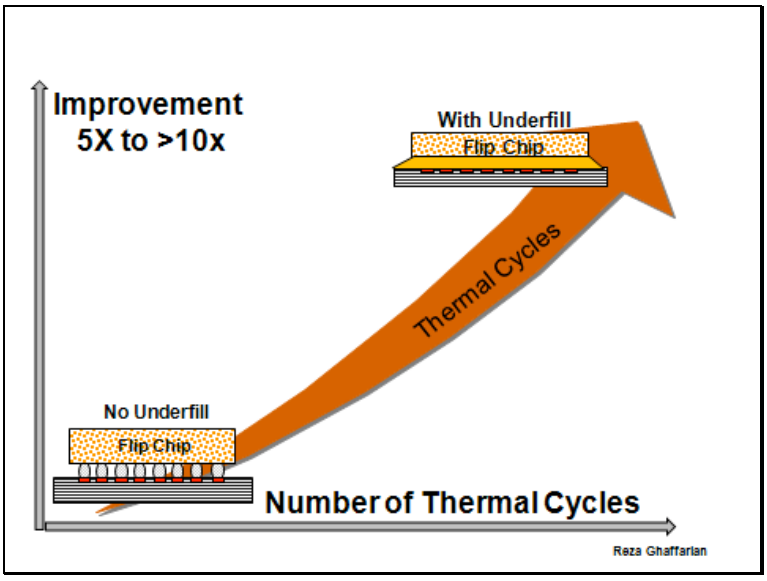

Figure 2. Underfill enables the use of large flip-chip die and polymeric substrates, because it significantly improves resistance to thermal cycling.

Emphasis is placed on board-level reliability due to underfilling. At the board level, key parameters that influence the thermal cycle and mechanical reliability of underfill, edge-bond, and corner stake are discussed in detail using literature surveys and recently presented conference papers. Particularly, thermal cycle and mechanical reliability data are presented for fine pitch ball grid array (FPBGA) and ceramic BGA assemblies. Figure 3 shows the level of improvement in mechanical fatigue resistance with package underfilling. There is enough moderate improvement to meet less stringent requirements for number of 'drops to failure' for commercial applications. Note the positive and negative arrows showing the thermal cycles for underfilled conditions. At the package/assembly level, underfilling may have negative effects on thermal cycle reliability if there is not an appropriate CTE match to adherents with enough stiffness rigidity. Understanding key characteristics of underfill materials, as well as the process and quality assurance indicators for reliability, is important to prudently selecting and narrowing the follow-up test methods in preparation for low-risk insertion of advanced electronic packages.

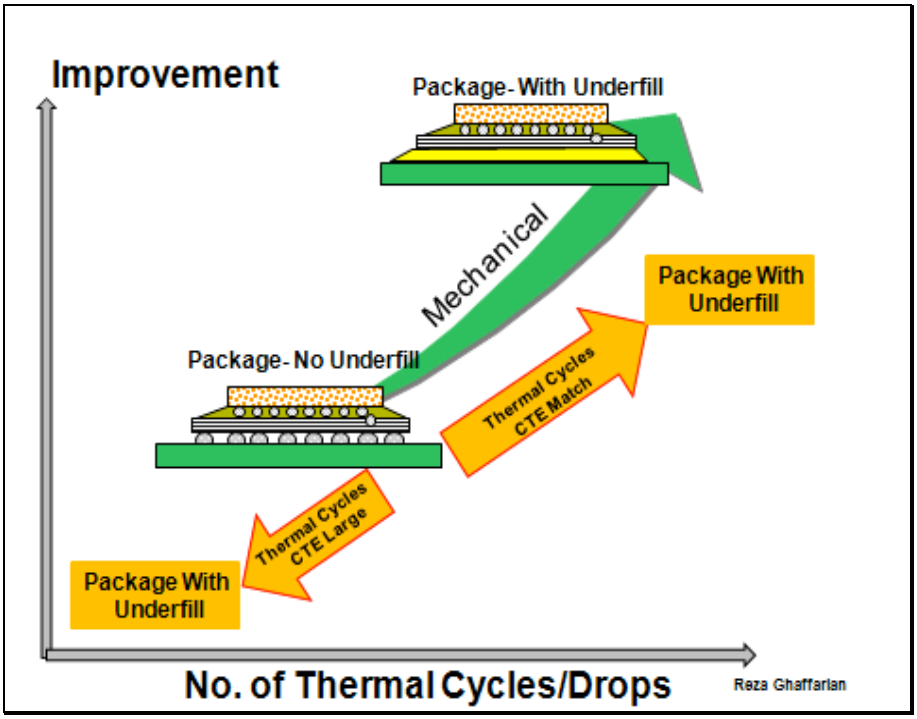

Figure 3. Underfill generally improves the mechanical resistance of package/assembly. However, thermal cycle resistance of package assembly may or may not be improved with underfilling. Large CTE mismatch underfill generally have negative effects on resistance to thermal cycling.

2. Electronics Packaging Trend

Contrary to early microelectronic technologies that aimed mostly at meeting high-reliability applications, now consumer electronics is driving the trends for electronic packaging and assembly. With that being the primary driver, materials and processes are transitioned to Pb-free solder alloy due to implementation of restriction of hazardous substances (ROHS). While there is a drive to develop new low-k dielectrics and advanced organic substrate materials, the higher melting temperature of these solder alloys is pushing the limits of the reliability. High-reliability industry now uses specialty electronics and either adapted consumer electronics or their own tailored versions.

In the past, for high-reliability applications, there was always ceramic versions of plastic packages, such as the plastic ball-grid-array (PBGA) and its analogous ceramic ball-grid-array (and column-grid-array) (CBGA and CGA). Today there are fewer ceramic versions, generally utilizing an older technology, available for harsher environmental applications. In fact, under thermal stresses, even though ceramic packages are individually more reliable compared to their plastic BGA versions, they may not always be the most reliable choice when assembled onto polymeric board due to a much larger coefficient of thermal mismatch. Solder joint reliability under thermal stress, especially thermal cycling, has become an integral part of the microelectronic packaging equation for overall system reliability, especially for high-reliability applications [1-8].

The trend in single packaging technology is illustrated in Figure 4. Single chip packages such as BGAs and CSPs (chip scale package) are now widely used for many electronic applications, including portable and telecommunication products. The BGA version is now being considered for high-reliability applications with generally much harsher thermal and mechanical cycling requirements than those for commercial use. Technical challenges for BGA/CSP packages, including the behavior of solder joints under thermal and mechanical loading, have become a ‘moving target’ to meet development requirements in higher density die with its associated continuously increase in pin counts (I/Os), decreasing in pitches, and newly introduced packaging styles.

For high-reliability applications, thermal stress is a concern as the I/O of CGA packages increase and the package itself becomes more complex, with exposed flip-chip die as a non-hermetic feature and added passives on the package substrate. Thermal stress due to column attachment for LGA and/or reworked CGA packages affects reliability. Assembly of LGA directly onto board using conductive adhesive may become a viable option in the near future, possibly using adhesives with nano-particulates or other approaches. Thermal characterization of early versions of high I/O PBGAs with wire bond, as well as advanced higher I/O version with flip chip die, is critical for certain harsh environmental applications. Evaluation of CSPs, including wafer-level CSP (WLCSP), should be selective since packaging technologies don’t yet show the thermal resistance robustness required for high-reliability applications.

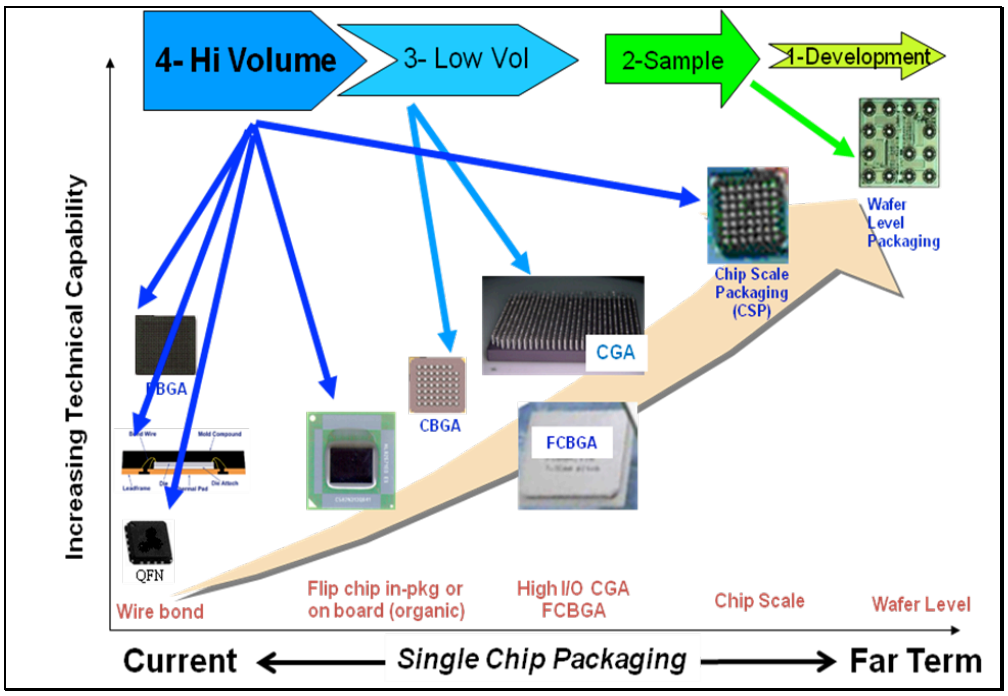

Figure 4. Microelectronic trends for single packaging technologies.

With a majority of commercial industry already implementing Pb-free solders in their products, there is now added complexity and challenge for high-reliability applications. The options for users of tin-lead solders are (a) continue to use tin-lead solder with Pb-free columns/solder balls (backward compatibility), (b) replace Pb-free balls/columns with tin-lead, or (c) accommodate Pb-free in the near future with an understanding of associated risks and continuing to develop mitigation approaches. Underfill has been used for flip-chip die in high I/O CGA and BGAs. However, the question of using underfill at the package level remains to be fully investigated by testing to determine their wider suitability for high-reliability applications.

3. Underfill Applications

3.1 Adhesives Types

Polymeric adhesives, both insulative and conductive types, are widely used in the assembly of devices, packages, and PCBs. For example:

- Attachment of bare die with thermally conductive adhesive for the purpose of bonding and heat dissipation
- Underfill adhesive filling the space between flip-chip die and substrate to absorb thermal stresses and relieve thermal load on solder interconnection
- Anisotropic conductive adhesive (ACA) replacing solder interconnection, especially in the era of Pb-free
- Corner staking of large ceramic quad flat packages for mechanical strengthening of fragile solder

For the mobile industry, use of full and edge underfill of advanced fine pitch BGA (FPBGA) and stack packages, such as package-on-packages (PoPs), are now commonly used to increase resistance of assemblies to repeated drops, a new requirement for mobile electronics applications. Adhesives in electronics assemblies are categorized based on their physical forms, polymer types, formulation, curing method, function, or intended applications.

Figure 5 summarizes the first three key categories of adhesive characteristics along with their subdivisions in each category [9]. Adhesives are available in all physical forms—solid, liquid, and paste. For use in electronics assembly, flow of liquid adhesives and paste are controlled for accurate volume dispensing and for avoidance of further spreading during the solidification process. Flow is tailored by adding minerals and thixotropic compounds, such as silica powder, enabling ease of dispensing by syringe or squeezing through stencil for adhesive paste printing.

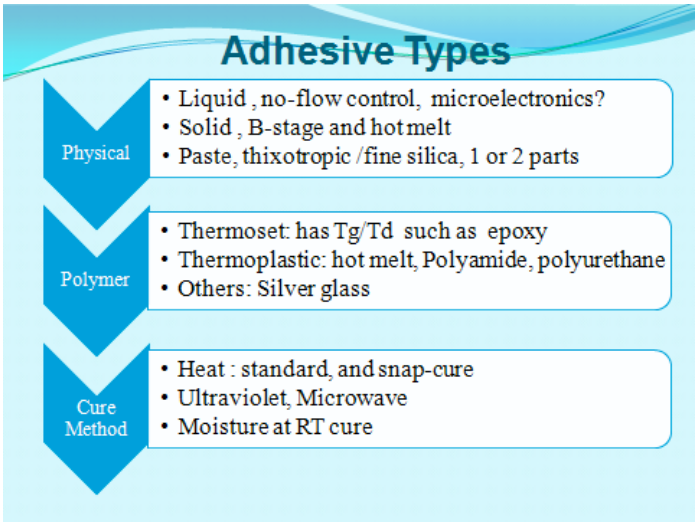

Figure 5. Key classifications of adhesives and their cure methods.

Paste or liquid adhesives are either one-part or two-part types. The one-part version is cured upon exposure to appropriate curing methods, whereas the two-part version—one part adhesive with the part hardener or catalyst—requires admix of the two parts (A and B) before their cure and use. Separation of A and B in thermosetting polymer allows for long-time storage of adhesives and use as needed by mixing the two parts. This is not the case for thermoplastic adhesive, since the polymer melts or flows at specific temperatures or within temperature ranges, and then re-solidifies upon cooling.

Epoxy polymer adhesive is a good example of the thermoset category, with a glass transition temperature (T_g) at the region where changes in behavior occur. Thermoset adhesives also have a decomposition or char temperature (T_d), not melting or exhibiting plasticity as is the case for thermoplastic polymers, such as polyurethane and polyamide. There are other types of adhesives that do not fall within these two key categories (thermoplastic and thermoset). For example, silver glass is a non-polymeric adhesive paste consisting of glass with silver particles, a polymer binder, and a solvent. Exposure of polymer binders to high temperatures (400–450°C) during processing causes burn-off the polymer binder, melts the glass, and fuses the glass and oxide, completing the curing process.

Curing of polymeric adhesives is not limited to heat only. Curing is performed using other types of energy applications as well. Key curing methods are:

- A widely used curing process is accomplished with conventional heat. Heat process optimization is narrowed using analytical test methods such as thermo-mechanical analysis (TMA) or differential scanning calorimetry (DSC). For rapid cure in mass production, snap-cure adhesives are developed (generally cyanate ester) that cure in less than one minute's time at higher temperatures.
- Ultraviolet (UV) curing of adhesives is widely used because of its rapid cure time (in seconds, vs. hours for thermoset), and there is no need for heat energy. UV-cured adhesives are used for positioning and bonding precision parts, such as fibers in optoelectronic circuits.
- The variable-frequency microwave (VFM) curing process is 2-10 times faster than conventional heat curing.
- Moisture curing of adhesives requires only ambient moisture, however, it takes days to cure completely and short exposure to high heat may be required to accelerate the process.

3.2 Thermoset Adhesive and T_g

For thermoset polymeric materials, there is a transition temperature (T_g) or temperature region where polymer changes from a rigid, glassy state to a rubber-like, soft amorphous state. This transition region is associated with molecular changes from a somewhat ordered to a more random state of high molecular motion. T_g is measured by various methods. One method detects transition in expansion by graphically plotting the expansion of polymeric materials as a function of temperature, the narrow region where significant changes in expansion occurs. The changes in CTE in this region could be high enough to cause users to be aware of major changes in state of stress. T_g is the single-

point temperature that corresponds to the intersection of lines drawn tangentially to the glassy and robbery regions (i.e., in the graphs showing CTE with temperature variations).

In general, T_g values well below RT define softness, the domain of elastomers, whereas values above RT define rigidness, the domain of structural polymers. It is critical to have knowledge of T_g in order to select the right underfill—not only for its thermal limitations, but also its CTE value relative to die, package and PCB (for its compatibility with adherents). Figure 6 shows a sample T_g for a PCB, defined by intersection of the two tangents drawn at the low and high CTEs [10].

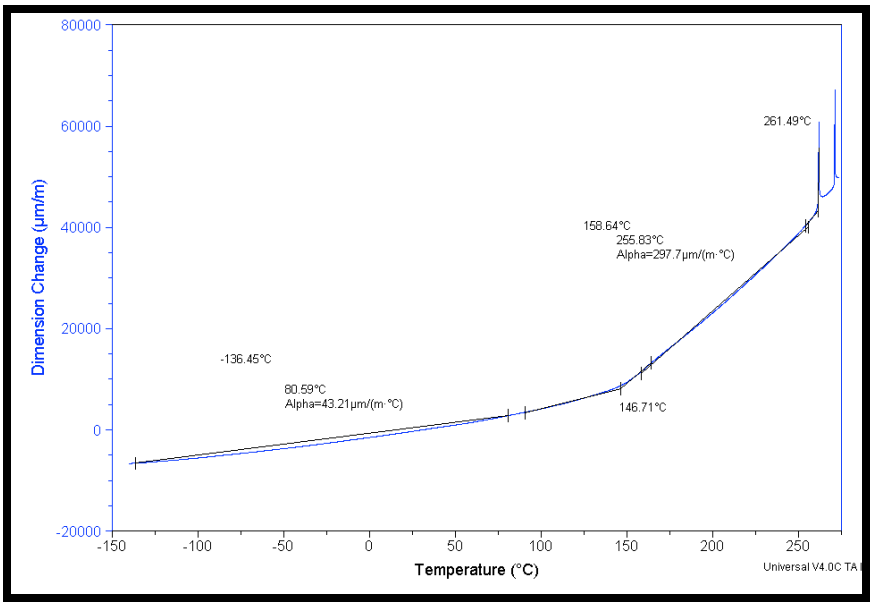

Figure 6. Glass transition temperature measurement (Tg) by dimensional change for a printed circuit board in the z-axis (R. Ghaffarian, Reference [10]).

Characterization of the viscoelastic properties with temperature can also be used to determine T_g using the dynamic mechanical analysis (DMA) method. A sinusoidal force (stress) is applied to the material at a set frequency and the response (strain) to this input is measured. The ratio of peak stress to peak strain gives a complex modulus from which storage modulus (G') and loss modulus (G") are obtained. The storage modulus is related to the energy stored by the material per cycle.

Figure 7 shows a storage modulus curve for a widely used polymeric adhesive tested from −130ºC to +150ºC at a constant frequency (1 Hz) and constant amplitude (50 μm), using the TA Q800 DMA instrument [11]. Stiff and glassy materials have a high storage modulus. The loss modulus is related to the energy dissipated by the material during the cycle, and it will go through a significant decrease in the peak Tan Delta (Tanδ) region of the sample. Tanδ is the ratio of the loss modulus to the storage modulus and is commonly referred to as the loss factor. It is related to the viscoelasticity and damping (how well the material can disperse energy) of the material. The maximum in the Tanδ peak, as well as intersection of the line tangent to the loss modulus lines, are also reported as the glass transition temperature.

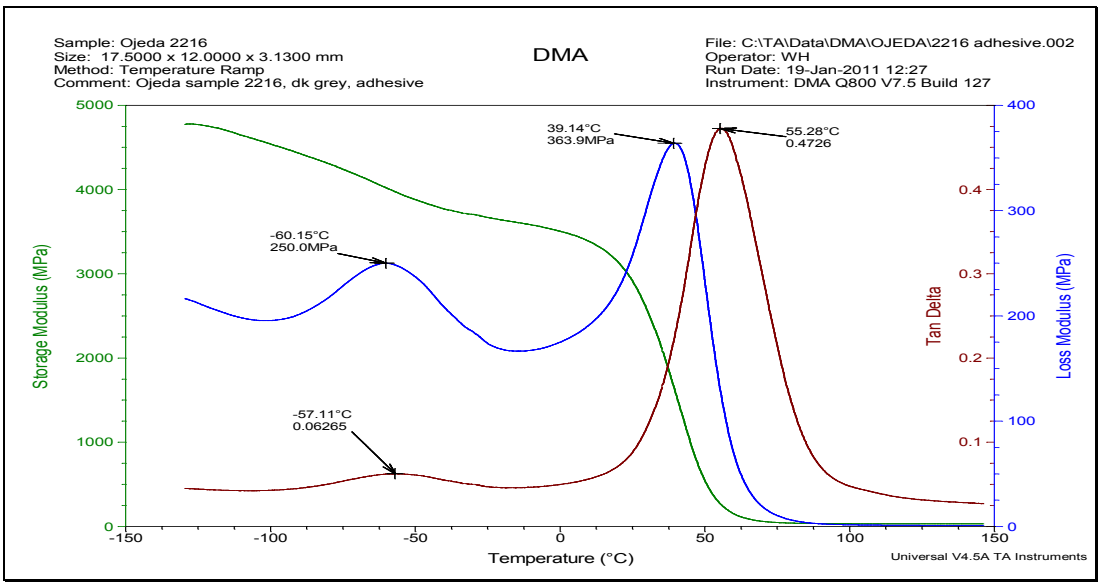

Figure 7. Example of dynamic mechanical analysis (DMA) for a polymeric adhesive tested from –130ºC to +150ºC (Ojeda, C.E., et al, Reference [11]).

3.3 Adhesives Function and Underfill

Figure 8 shows additional classifications of polymeric adhesives based on functional use, intended application, and surface mount technology application, especially when underfill is used at the part and the package levels. Adhesives perform various functions including mechanical attachment, electrical connection, and as thermal and mechanical stress dissipater.

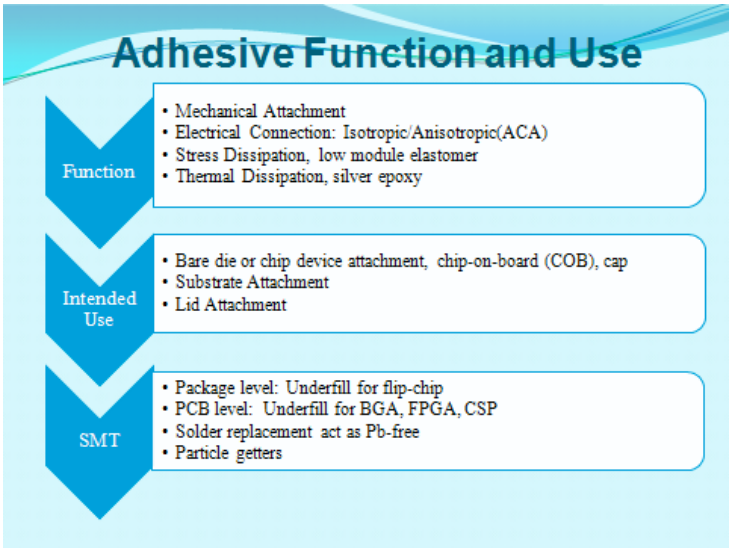

Figure 8. Key adhesive functions and their use.

When two dissimilar materials are mechanically attached, there must be sufficient shear and tensile pull strengths to adequately maintain strength during its lifetime exposure to thermal cycling, aging, moisture, and other environmental requirements. For flip-chip die, since underfill adhesive covers the whole area under the die, stress is dissipated away from the finer solder ball interconnections. Electrical attachments, replacing the electrical function of solder or wire, are accomplished by isotropic or anisotropic (z-direction only) adhesives. Metallic fillers, e.g., silver in epoxy, provide conductivity. Metallic fillers also act as heat dissipation agents; therefore, the attachment has the benefit of heat conduction.

For hybrid and multichip packaging technology, adhesives play a significant role in both providing the electrical connection and providing enough mechanical strength to resist mechanical loading, such as that induced by shocks and vibrations. Bare die attachment is accomplished with non-conductive adhesive; chip attachment (such as chip resistors and capacitors for interconnection attachment) uses conductive adhesives. Tin-film and thick film could also play a role when using adhesives for substrate attachment. Hybrid-package lid could be attached using adhesive even though they do not have an ideal sealing capability.

For SMT, adhesives as underfill are used to fill the gap between the die and substrate for flip-chip attachment within packages and for filling between packages and PCB for area array packages. Underfill at the package assembly level is a newer process that is being developed to compensate for finer pitch array packages, which show much lower resistance to mechanical and fatigue loading. The critical function of underfills, chiefly at package assembly levels, is further discussed.

3.4 Underfill for Flip-Chip Die

For surface mount technology, adhesives have been widely used for the die attachment and over molding. During the early development of flip-chip technology, it was recognized that underfill is required to improve solder joint reliability. Without underfill, the solder joints failed by induced thermal stresses due to coefficient mismatch of die and ceramic substrates. The need for underfilling become more critical when substrates changed from lower CTE ceramic to higher CTE polymeric materials and the size of die increased; therefore inducing much higher stress on solder joints.

In 1997, an experimental study, combined with parametric modeling life cycle projection for various ceramic die on ceramic substrate, documented the effect of various parameters caused by thermal cycling CTE mismatch [12]. Figure 9 clearly shows the dependency of life on die size, indicated by the distance to neutral points (DNP) for a non-underfilled condition. This is not true for the underfilled condition. In the plots, open circles indicate points generated by modeling and closed squares represent experimentally measured data points. Thermal cycling carried in the range of –50°/150°C and –40°/125°C.

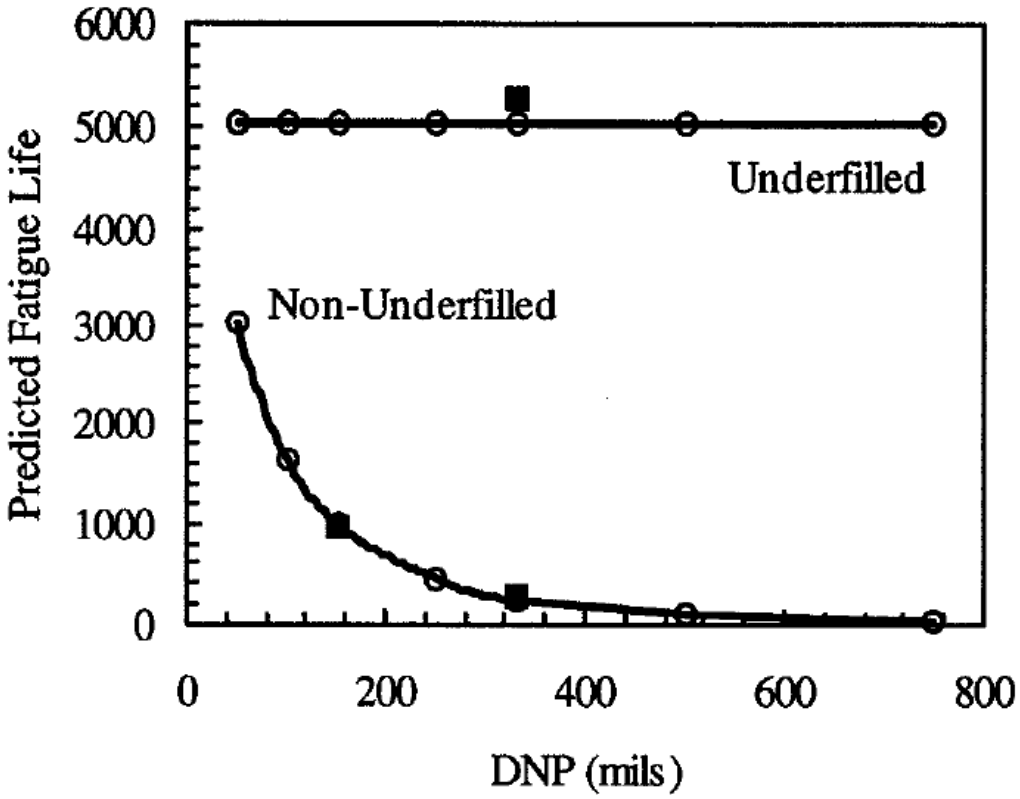

Figure 9. Underfill shows thermal cycle fatigue life improvement and no change with change in die size, shown as the distance to neutral point (DNP) (See S.F. Popelar, Reference [12]).

At the IEEE ITHERM conference in June 2012, experimental test results with modeling were presented showing the effect of underfill type on the reliability of flip-chip die technology with copper-post (pillar) solder joint interconnection [13]. Note that Cu-pillar bumping is known to possess good electrical properties, better electro-migration performance, and better thermal fatigue resistance. The drawback is that Cu-pillar bump can introduce high stress due to the higher stiffness of Cu compared to the solder material. Test conditions for Cu-pillar with underfill evaluation included having a flip-chip die on FR4 with a Cu-pillar/bump size of .04 mm, pitch 0.1 mm, chip thickness of 0.79 mm, and PCB thickness of 1 mm. The behavior of each underfill with temperature was evaluated by DMA and digital image correlation (DIC) images, and modulus and T_g values in particular were considered as indicators for their effectiveness in improving reliability.

Table 1 lists the experimental test results, including T_g and cycles to failure for a thermal cycle profile in the range of 0° to 125°C (5 minutes ramp and 10 min dwells). The sample without underfill failed at less than 100 thermal cycles. Theoretically, modeling indicates that those with underfill should show significant improvement (in the range of 10- to 100-fold). Experimental results, however, showed up to 20-fold improvement for underfill D with the highest T_g value.

Table 1. Summary of test results for flip-chip die with and without underfill.

Flip-Chip Condition	Tg	CTE1	CTE2	TC (0/125°C) Failure Model	TC Failure Experiment
No Underfill	NA	NA	NA	**63**	**75**
Underfill A	110	57	145	1228	1050
Underfill B Reworkable	80	30	87	1716	NA
Underfill C	125	30	86	5476	NA
Underfill D	150	33	87	**6110**	**> 1500**

Piezoresistive sensors were used to characterize the in-situ die surface stress evolution during thermal cycling of a flip-chip ceramic ball grid array (FC-CBGA) package [14]. The test chips had dimensions of 20 × 20 mm, and 3600 Pb-free solder interconnects (full area array) were used to connect the chips to the high CTE ceramic chip carriers. Before and during packaging steps, including flip-chip solder ball reflow, underfill dispense and cure, lid attachment, and adhesive cure, the sensor resistances were monitored to document stress on die during assembly operations. It was observed that the majority of the die compressive stress was accumulated during the underfilling assembly step. Typical increases in the stress magnitude were on the order of 300% (relative to the stresses due to solder joint reflow only). .

A package carrier was developed to allow measurement of the die stresses in the FC-CBGA components that were subjected to thermal cycling loads without inducing any additional mechanical loadings. Cycling was performed in the range of 0° to 100°C (40 minute cycle, 10 minute ramps and dwells). Initial fluctuations in stress values preceded a trend of constant stress values on the die for up to 9,000 thermal cycles. No data was generated for flip chip with no underfill, but clearly the test results indicate the significant effects of underfilling on uniform distribution of stresses, even at the edge of the die.

3.5 Underfill for Array Packages

Contrary to flip-chip die where underfilling is regularly required, the area array packages on PCB underfilling is selectively performed on rare occasions due to increases in cost, added process steps, and hindered reworkability. Underfilling is performed only for critical applications with severe environmental requirements. However, similar to flip-chip die in package, flip-chip assembly on PCB is also often required to be underfilled due to the large

CTE mismatch between ceramic die and polymeric PCB. For plastic ball grid array, chip scale package, fine pitch BGA, and wafer-level package assembly onto board, underfilling is generally required when assemblies are exposed to a large number of repeated mechanical loadings during application. With the advent of portable electronic applications, underfill is often considered for these types of packages to improve resistance to potential repeated drops during their life usage.

Reliability improvements achieved with underfill need to be considered against added throughput, cost, and reworkability. The CTE of underfill also needs to be considered. The effect of underfill on reliability improvement can be optimized by varying the amount of filler additive used to modify the CTE of underfill materials (e.g., to better match adherent substrates and solder joint CTEs). To reduce process steps and compare cost with standard underfilling after assembly, new underfill materials have been developed that, added early during solder joint assembly and fully or partially, cure at the time of solder joint reflow and assembly. This is called no-flow underfilling, and is different than the capillary process commonly used in a other process steps. Figure 10 is a schematic diagram of process steps for both capillary and no-flow underfills. Reworkability has been eased by developing re-workable underfill.

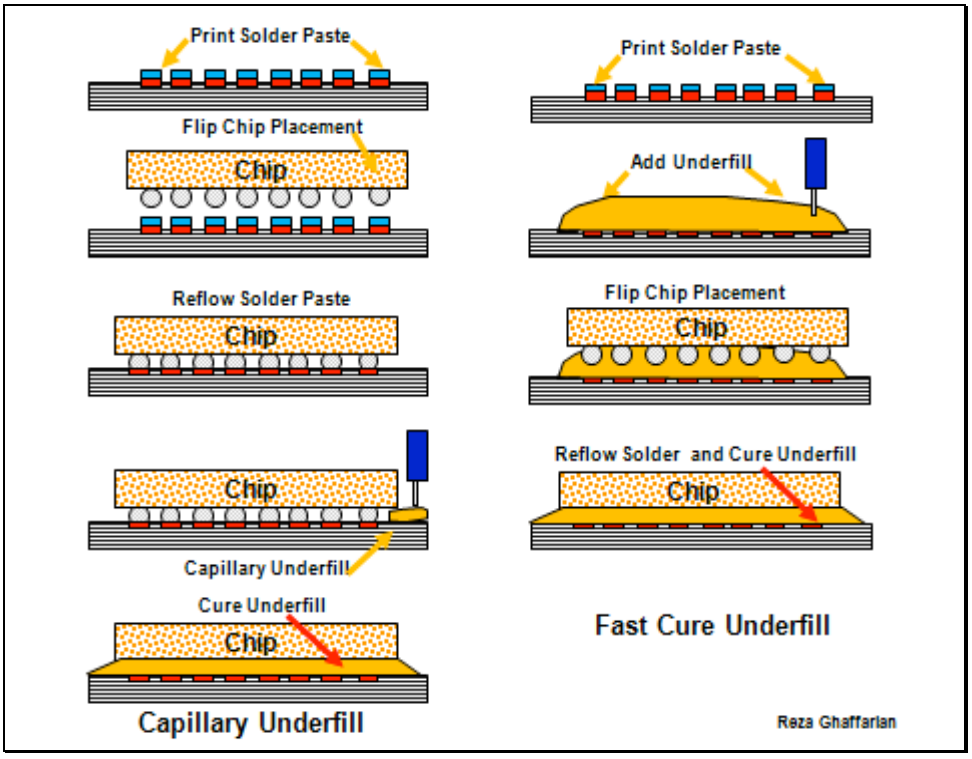

Figure 10. Capillary and no-flow underfill process steps and applications for flip-chip die.

The capillary underfill process has been widely used for underfilling at the die, flip-chip, and board levels for CSP and FPGAs. This process is typically done one device/package at a time and is considered to pose throughput limitation. Modern dispensing equipment is highly flexible and can be quickly reconfigured for adjustment to the process or product. The flow

of underfill relies on the capillary forces between device/substrate and package/PCB, as well as the fluidity flow of the underfill in filling existing gap height and traversing die length. The type and amount of filler in underfill not only affects CTE, it also affects fluid flow under the die and, therefore, filling integrity and processing time need to be considered when optimizing underfill materials. Capillary action is also affected by adherents including die passivation, solder mask, package substrate surface, and PCB surface and condition; these variables can either help speed the flow or impair it. Surface cleanliness is also important; for example, flux residue hinders flow if not cleaned properly.

There is concern that capillary underfill may reach its limitation as die thickness significantly decreases, the interconnection (bumps/pillar) get smaller, and the number of bumps increases. In an experiment, capillary underfill was injected into the fine gap (75 to 300 μm) of a sample made of glass plates mounted on organic boards [15]. The surface of the board had different topographies including grooves of different depth and widths, as well as holes drilled to different diameters and depths, from 250 μm to 1.5 mm. When groves are parallel and narrower compared to the gap, voids are formed. However, for the case of grooves normal to the fluid flow, voids are not formed independent of the groove geometry. For a very deep groove, the flow will simply cease to continue. The author concludes that in future packaging design, rules need to include the capillary physics present during underfilling and fluid dispensing.

No-flow underfill is implemented to speed the process and cut the number of heat steps and equipment use. Basically, it uses a chemical process to accomplish several operations. Underfill added prior to placement of flip-chip die functions simultaneously as flux and cure. Then, during reflow, it solidifies while cooling, in the same manner as solder interconnections. Since underfill and array packages simultaneously cure/reflow, this limits the robustness of array packages by self-alignment and heightens the need for more accurate placement of packages on PCB. In some cases, it may be necessary to hold parts down during reflow/cure. No-flow materials have no filler particles to modify the resin, and a CTE of 70 ppm is typical. Large CTE underfill is not suitable for flip-chip application; it is more appropriate for array package on-board underfilling.

Capillary underfill generally uses thermoset polymers, so there is no simple rework of the parts—by definition thermoset polymers do not soften with heat. Several underfill material suppliers have created reworkable underfills that decay or softer with heat. Reworkable underfill generally uses standard dispensing, with capillary flow for pull the fluid under the part.

3.6 Specifications on Adhesive and Underfill

Although epoxy adhesive has been around since 1930, the first specification for the qualification of adhesives was issued by NASA Marshall Flight Center in 1978 [9]. Earlier adhesives had some major issues, including ionic impurities and organic trapping under large die. In the 1980s, concurrently with IC device refining and development, the third generation of adhesives emerged, made with high purity, low ionic content, and no-solvent (including epoxies and polyimide). Interest was renewed for their use on flip-chip devices for high speed circuits and high I/Os. Underfill was introduced to fill the gap within flip-chip adherents and to dissipate large stresses due to CTE mismatches. Also, high-density

multichip packages were introduced that use different adhesive types. The fourth generation of adhesives, developed in 1990s, were specifically formulated with low moisture absorption, high thermal stability, and low stress to be compatible with reflow soldering. They were developed to prevent or reduce the 'popcorn effect', which is attributed to rapid release of water absorbed in adhesive and molding compounds on the exposure to high-SMT solder-reflow temperatures. The requirement for high-throughput automated assembly resulted in the wide use of adhesives with rapid curing characteristics, such as snap-cure adhesives and fast capillary flow underfills.

The NASA MSFC specification was further revised and released in 1982, SPEC-592, "Specification for Selection and Use of Organic Adhesives in Hybrid Microelectronics." Later, all government specifications were administered by the U. S. Air Force at Rome Air Deportment Center. Now, Method 5011 of Mil-STD-883 covers qualification of adhesives, as well as other polymeric materials for use in high-reliability electronic applications. Defense Supply Center, Columbus (DSCC), Ohio, who administered Mil-STD-883, was recently was renamed as defense logistics agency (DLA) for Land and Maritime.

The commercial industry specification J-STD-030, "Guideline for Selection and Application of Underfill Materials for Flip Chip and Other Micropackages," addressed polymer-based underfill materials intended for use in electronic packaging assembly applications. Underfill relieves stress on joints that interconnect flip-chips, chip scale packages (CSP), and ball grid arrays to an interconnection substrate. Types of underfill materials covered by this specification are: capillary flow, no-flow, and reworkable underfill. The specification does not cover molded or wafer application underfills.

To address the use of advanced non-hermetic flip-chip package in high pin count CGA packages, a new Class Y is being introduced into the qualified manufacturer list (QML) system. Class V is not appropriate for this category of packages because that classification is intended only for hermetic devices. The diagram in Figure 11 shows recent class Y activities and accomplishments, and was presented at the NASA Electronic Workshop, June 2012 [16].

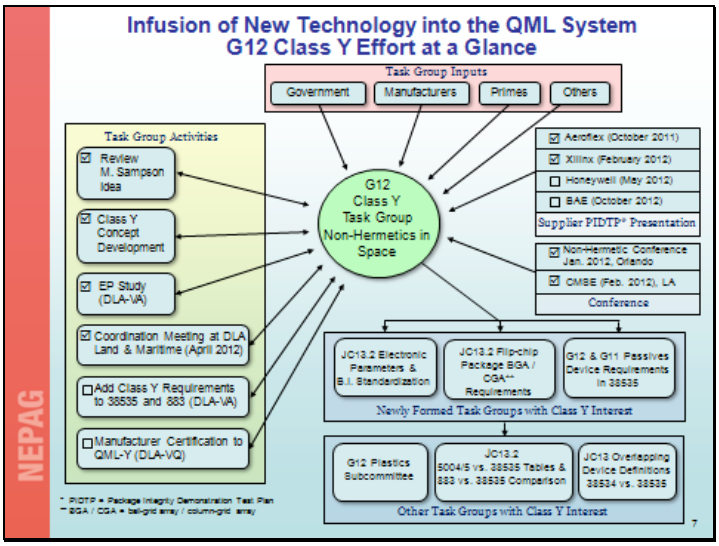

Figure 11. Class Y activities eligible for inclusion in non-hermetic flip-chip packages (listed in the qualified manufacturer list (QML) system).

4. Test Data on Reliability

4.1 Introduction

Reliability is the capacity of a system (here microelectronics) to function as expected under the expected operating conditions, for an expected time period, without exceeding the expected failure levels. However, reliability is threatened by infant mortality due to workmanship defects and the general lack of sound manufacturing and reliability design. Designs for manufacturability (DfM), design for assembly (DfA), design for testability (DfT), and so on, are prerequisite to assure reliability of the product. Only a design for reliability (DfR) can assure that manufactured to quality will be reliable. The elements of system reliability (Figure 12) are the device/package/PCB and its interconnections, but also includes consideration of design for reliability prior to assembly and subsequent manufacturing and quality assurance implementation.

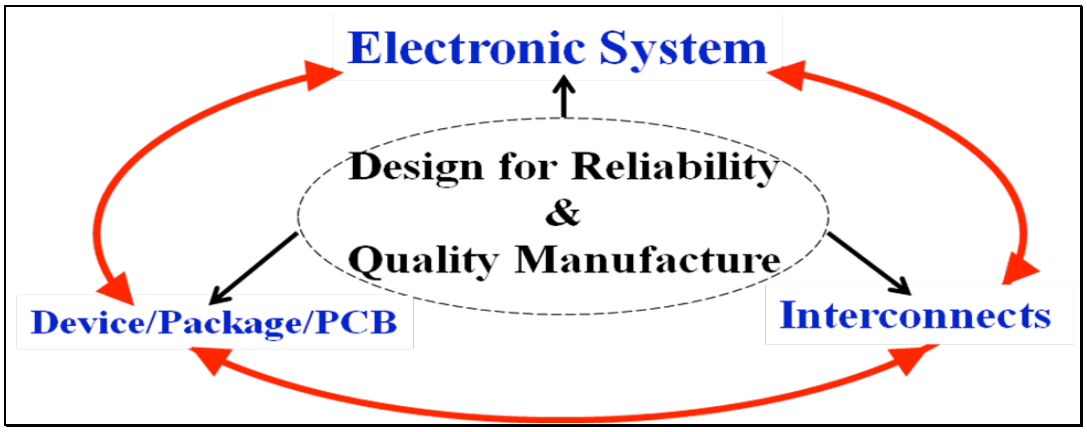

Figure 12. System reliability achieved through design for reliability (DfR), sound manufacturing, and quality of packaging/device/PCB and interconnections.

Even though underfill has numerous drawbacks, its key role is to improve reliability by dissipation of stress away from the weak interconnects without introducing other unwanted failures. To achieve higher reliability and proper use of underfills, it is critical to understand all stresses induced during processing of underfill, generally noted by residual stress, and any subsequent environment exposure, defined by fatigue behavior. Stresses induced during process could cause cracking of the die and package and failure of interconnection due to overloading. On the other hand, fatigue failures are induced due to repeated thermal cycling or mechanical loading exposures. Physics-of-failure for each case is different and in some cases may contradict each other. In that case, a compromised optimization may be required for their effectiveness. The key findings on parameters affecting reliability with underfill are discussed in the following sections.

4.2 Residual Stress Due to Underfill

Residual stress is due to resin shrinkage during curing and resin polymerization during cool down to room temperature. In its simplest form, the stress induced is proportional to the

adhesive modulus and thickness and inversely proportional to the radius of curvature, which is related to warpage. Therefore, warpage after curing and subsequent steps may be used as a quality indicator for the level of residual stress. If CTE mismatch is considered, thermal stress induced on die/substrate/adhesive depends on CTE of adherent, size of die, thickness, and modulus of elasticity. For example, because of the much larger CTE of underfill relative to Si/substrate in the flip-chip die assembly, stress on die becomes compressive due to resisting larger shrinkage of underfill during cool down from cure temperature. In this case, adhesive is under tensile stress. A relationship between various properties of rectangular die and underfill is shown in equation 1 [17].

$$S_{max} = K (\alpha_{Sub} - \alpha_{Si}) (T_o - T) \sqrt{(E_a E_{sub} L/\chi)} \quad (1)$$

Where S_{max} is the maximum stress, K is a geometric constant related to shape and filleting, α_{Sub} is the CTE for substrate, α_{Si} is the CTE for Si die, E_a is the modulus for adhesive, E_{sub} is the modulus for substrate, L is the length of die, χ is the thickness of adhesive, T_o is the cure temperature , and T is the use/exposure temperature.

4.3 Thermal Fatigue

Reliability under thermal stress for package and assembly depends on the reliability of constituent elements and global/local interfaces (attachments) [18]. Solders in surface mount are unique, since they provide both electrical interconnection and mechanical load-bearing elements for attachment of the package on PCB, and often function as a critical heat conduit too. A solder joint in isolation is neither reliable nor unreliable; reliability has meaning only in the context of interconnections, either within package or outside of package on PCB. Solder joints are a key interface element for FBGA packages and assembly on PCB. Three elements play key roles in defining the reliability for FPBGA/FCBGA: global, local, and solder alloy. In FBGA, solder balls also act as a load-bearing element between package and boards, similar to metallic leads like those for QFP. The characteristics of these three elements—package (e.g., die, substrate, solder joint, underfill), PCB (e.g., polymer, Cu, plated through hole, microvia), and interconnections (e.g., solder joints, via, balls, underfill)—together with the use conditions, the design life, and acceptance failure probability for the electronic assembly, determine the reliability of advanced area array electronic packaging assemblies (with and without underfills).

4.4 Mechanical Fatigue

Area array packages, in general, and flip-chip dies and FPBGA specifically, lack the thermal and mechanical resistance generally observed for PTH and leaded package assemblies soldered with $Sn_{37}Pb$ alloys. Lack of reliability resistance is further aggravated with the use of lead-free solder alloys, especially under harsh thermal cycling and dynamic loading, such as drop and vibration. For these reasons, underfills were used in industry to improve solder joint reliability of finer pitch area array package assemblies during early implementation of this technology, even when use of tin-lead solder alloys was common. Underfill is used both within packages and on the PCBs. It acts to absorb

the CTE mismatch, which reduces stress significantly by distributing it uniformly through the solder joints.

Underfilling does have undesirable qualities: additional process requirements, increased cost, and reduced manufacturing throughputs. Another drawback of underfill is the inability to rework defective parts. Progress has been made to reduce the negative impact of underfilling by shortening the process time though the use of snap cure polymers and enabling reworkability by the development of reworkable underfills. So, if it is generally accepted that underfill improves reliability, then one might think that if everything else failed to improve the reliability of array packages/chips, underfilling might be the ultimate undesirable solution. Indeed, CSPs were undefiled when passport-size cameras were introduced for the first time in early 1997, possibly to expedite use of CSPs and eliminate their potential early failures since at that time CSP's long-time behavior, especially under use condition, was not yet well understood.

4.5 CSP and FPBGA—Literature Reliability Test Data

Extensive work has been carried out by various investigators to address the effect of underfilling on the weakness of area array packages under mechanical loading and the improvement achieved by underfilling. The few instances of the investigation that are discussed here hope to shed some light on the effects of key parameters that affect reliability both under thermal cycling and mechanical loading. For example, in reference [9], written in the early stage of introducing portable electronics, it states that thermal cycle reliability has been shown to meet many consumer application requirements. However, fine pitch BGAs and CSPs have difficulty meeting mechanical shock and substrate flexing tests for portable electronics applications. Underfills are being used to improve the mechanical reliability of area array packages.

Test vehicles included 4 FPBA (with 108 balls and 0.8 pitch), a 10 × 10 mm package with 5x5 mm die that were assembled on a 0.039-inch PCB with fast curing and reworkable underfills. Assemblies with the reworkable underfill were reworked to determine the issues with reworkability and its effect on reliability. The test vehicles were subjected to thermal shock cycling, drop, and flexing. Thermal shock cycles were in the range of –40° to 125°C, with 1 minute transition time and 5 minute dwell at the extremes. A total of ten drops from a height of 6 feet were performed. Repeated flexure testing was also performed at twice the radius, which caused failure of the board during monotonic bending (17.5 and 8.76 inches). Test conditions and results are summarized in Table 2. Even though test results for thermal shock did not show a clear trend, significant improvement in mechanical performance was achieved with both the reworkable and the non-reworkable underfills. The reworked process did not degrade mechanical performance—it improved it. The use of underfill did not alter thermal shock performance. Excessive voids thought to be due to flux residue; it decreased with use of reflow in a nitrogen atmosphere.

Table 2. Summary of test results for FPBGA, with and without underfill.

FPBGA 108 I/Os 0.8 mm Pitch	Tg	CTE1 <Tg	CTE2 >Tg	TS Failure (-40/125°C)	10 Drops (6 feet)	Flex (1/2 max deflection)
No Underfill	NA	NA	NA	~1000	100%	113
Underfill A (3566)-Fast Flow	135 (DSC)	50	170	~1000 (voids)	No Failure	>1250
Underfill B (3567) Reworkable	94 (TMA)	65	190	>3000	30%	>1250
Underfill B-Reworked	94 (TMA)	65	190	NA	10%	> 5000

In a later investigation [20], the effect of corner bonding was compared to full underfilling on the resistance to the number of drops to failure for a tape array CSP package, 8-mm, 0.5-mm pitch, and 132 I/Os. Reading data from the failure graphs presented in the paper, it appears that at the 10 percentage failure line, no-underfilled assemblies crossed the failure line at 2 drops, corner bond assemblies at 5 drops, and full capillary underfill assemblies at 10 drops. The authors concluded that corner bond underfill provides a 3–4 times improvement compared to the no-underfill condition; therefore, corner bond underfill is a viable, cost-effective approach for many portable product applications.

Contrary to mechanical fatigue improvement with full underfilling, the effect on thermal cycling fatigue may be negative depending on certain properties of underfill, including CTE mismatch and modulus of adherents. In a recent study [21], it was shown that partial flow underfill covering corners had a relatively small negative effect on thermal cycle (–40° to 125°C) for two underfills with different materials characteristic. Of course, underfill can degrades thermal cycle resistance depending on underfill properties. The CSP package used in evaluation was 12-mm, 0.5-mm pitch, 228 I/Os, with 96.5%Sn/3.0%Ag/0.5%Cu (SAC305) Pb-free solder balls with 0.3 mm diameter. Board material was FR-4 and thickness was 1 mm.

To improve throughput and eliminate additional processing steps, preform underfill (underfilmed) materials were evaluated for BGA [22]. The materials can typically be provided in reels similar to discretes and placed around the perimeter of the BGA, following solder paste printing and prior to BGA placement. Similar to snap cure, it softens and cures during reflow and, by the conclusion of reflow, it is fully cured and remains adherent to both BGA and PCB. A number of test vehicles, assembled with 338 I/O 11 × 11 mm MAPBGA and 0.5 mm pitch using Pb-free SAC305 and preformed underfilm, were subjected to thermal cycling (0–100°C) and drop testing at 1, 500 g with 0.5 millisecond duration per JEDEC. No failure of assemblies to 3000 cycles and 100 drops were observed. Later drop g level

increased to 3,500 g in order to induce failures. Based on all test results, the author concluded that 8 times or more improvement in drop resistance at 3,500 g level is achieved when underfilm material is used. Underfilm showed no degradation effect in thermal cycling performance.

4.6 CBGA and CGA– Literature Reliability Test Data

For CBGA packages on board, because of a larger CTE mismatch than the plastic version, the negative effect of underfill on thermal cycling behavior may be more apparent. An investigation [23] was performed to determine the effects of various underfilling on CBGA package with 256 high-lead solder balls assembled onto PCB board with eutectic tin-lead solder. Test results for no-underfill and various underfills, cured at 165°C for 7 minutes, and their CTE and cycles brought to failure, are summarized in Table 3. It shows that underfilling CBGA can improve thermal cycle assembly reliability. However, a large CTE underfill can actually cause earlier failure than non-underfilled packages. A CTE almost matching the CTE for the solder joint alloy proved to be the most effective in improving board-level reliability. After 5,633 cycles of 0–100°C, no failures were noted for the CTE matched epoxy, whereas the other epoxies and the non-underfilled control parts had already failed.

Table 3. Summary of test results for CBGA with and without underfill.

CBGA 256 I/Os 1.27mm Pitch	CTE1	Young Modulus (E)	TC 1%Failure (0/100°C)	TC 63%Failure (0/100°C)	Model Project 63%
No Underfill	NA	NA	1980	2490	6690
Underfill A	75	2.6	931	2320	3690
Underfill B	44	5.6	3013	5420	7390
Underfill C	40	8.5	3100	5440	7630
Underfill D	26	5.5	> 5663	> 5633	9470

For CGA, including PBGA, the effect of corner staking with and without coverage on corner soldering has been reported previously, but recently the effect of adhesive properties (Tg and modulus) on edge-bonded CBGA was investigated [24]. Table 4 provides a summary of information on edge-bond properties as well as modeling information for Pb-free SAC387 and test results. Failures were from the package side at the corner balls for no edge-bond and edge-bond A epoxies, whereas failures were at the center balls away from the bond

for the edge-bond B epoxy. Edge-bond B epoxy with high modulus, lower CTE, and glass transition above 100°C improved the number of thermal cycles to failure (0–100°C), whereas underfill A epoxy had negative effects. The author explained that edge-bond adhesive play two roles: it resists expansion of the PCB; therefore, reducing stresses on solder joints and it lifts package corner away from PCB, increasing pulling stresses on solder joints. Stiff edge-bond adhesive with appropriate CTE should show the best results.

Table 4. Summary of test results for CBGA with and without edge-bond underfill.

CBGA 2400 I/Os 1 mm Pitch	**Tg**	**CTE1 <Tg**	**CTE2 >Tg**	**Δε %**	**ΔW**	**TC Failure (0/100°C)**
No Edge-bond	NA	NA	NA	0.608	0.111	786
Edge-bond A (E_a ~ 4000MPa)	30 (TMA)	65	136	0.852	0.168	629
Edge-bond B (E_b ~ 7000MPa)	100 (TMA)	32	106	0.492	0.087	2941

5. Conclusions

Since the inception of the first specification on adhesives by NASA's Marshall Space Flight Center (MSFC), the use of adhesive has significantly expanded. This is particularly true for portable electronics because of the special need to strengthen resistance to mechanical fatigue loading, such as repeated accidental drops by user. For high reliability applications, use of underfill is becoming extremely important, especially with the introduction of high input/output for non-hermetic flip-chip ball grid arrays and finer pitch BGAs. In lieu of full underfilling, partial underfilling or corner/edge-bonding, is a modified condition that may be sufficient for some uses. This BOK provided, through an extensive literature survey, the benefits and drawbacks of using underfill both for flip-chip die in packages and flip-chip BGA on PCB, as well as other advanced electronics packages and assemblies (board level).

At the board level, key parameters that influence thermal cycle and mechanical reliability of underfill, edge-bond, and corner stake were discussed. Particularly, thermal cycle and mechanical reliability data were presented for fine pitch ball grid array (FPBGA) and ceramic BGA assemblies. It is critical to bear in mind that at the package/assembly level, thermal cycle resistance may even decrease by corner staking, especially if solder joints are covered. Negative effects of underfilling on thermal cycle reliability is well established by numerous investigators for conditions with significant CTE mismatches.

A few key points on the effective use of underfill to minimize its negative effects, reduce stresses, and increase reliability (both mechanical and thermal) are:

- Use underfills with low shrinkage , low volatile condensation (CVM), and low TML (total mass loss)
- Reduce cure stresses by moderating the cure condition, e.g., use step cure or lower temperature cure
- Select underfills with CTE that closely matches CTE of adherents
- Choose underfills with low modulus of elasticity for low stress, but high modulus if higher strength in resisting to separation is needed
- Control disruption in induced stresses during operation or testing by selecting either T_g of underfill below or above the expected use temperature ranges
- Use corner and edge-bonding rather full underfilling for high reliability wherever possible. Underfill by capillary methods, since this process is well established.

Understanding key characteristics of corner staking/underfill materials, as well as the process and quality assurance indicators for reliability, are important in judicially selecting and narrowing the follow-up applicable test methods in preparation for low-risk insertion into advanced electronic packages. Prudent selection of underfill becomes more critical when used in advanced finer pitch and package-on-package technologies with lower resistance to thermal (and particularly mechanical) fatigue loading. It is recommended that users define a test matrix, using high reliability grade underfills and reworkable versions, to determine the key parameters for test vehicles built under high reliability conditions and for high reliability applications.

6. Acronyms and Abbreviations

ACA	Anisotropic conductive adhesive
BGA	ball grid array
BOK	body of knowledge
CBGA	ceramic ball grid array
CCGA	ceramic column grid array
CGA	column grid array
COTS	commercial-off-the-shelf
CQFP	ceramic quad flat pack
CSP	chip scale (size) package
CTE	coefficient of thermal expansion
Cu	copper
DfA	design for assembly
DfM	design for manufacturability
DfR	design for reliability
DfT	design for testability
DIC	digital image correlation
DLA	defense logistics agency
DMA	dynamic mechanical analysis
DNP	distance to neutral point
DOE	design of experiment
DSC	differential scanning calorimetry
DSCC	defense supply center columbus
EDX/EDS	energy dispersive x-ray
FPBGA	fine pitch ball grid array
FPGA	field programmable gate array
FCBGA	flip-chip ball grid array
HASL	hot-air solder leveling
HDI	high density interconnect
I/O	input/output
JPL	Jet Propulsion Laboratory
LGA	land grid array
MIP	mandatory inspection point
MSFC	Marshal space flight center
NASA	national aeronautics and space administration
NEPP	NASA electronic parts and packaging
NSMD	non solder mask defined
PBGA	plastic ball grid array
PCB	printed circuit board
PoP	package on package

PTH	plated through hole
PWB	printed wiring board
QA	quality assurance
QFP	quad flat pack
QML	qualified manufacturer list
RMA	rosin mildly activated
SEM	scanning electron microscopy
SMC	surface mount components
SMD	solder mask defined
SMT	surface mount
Tg	glass transition temperature
TMA	thermo-mechanical analysis
TV	test vehicle
QA	quality assurance
UV	ultraviolet
WLCSP	wafer level chip scale package

7. References

[1] Ghaffarian, R., "Reliability of Column/Board CCGA Attachment," *IEEE InterSociety Thermal Conference (ITherm)*, San Diego, CA May 31–June 2, 2012

[2] Ghaffarian, R., "Assembly and Reliability of 1704 I/O FCBGA and FPBGA," *IPC/APEX*, San Diego, CA, Feb. 28–March 1, 2012

[3] Ghaffarian, R., "Thermal Cycle and Vibration/Drop Reliability of Area Array Package Assemblies," Chapter 22 in *Structural Dynamics of Electronics and Photonic Systems*, eds. E. Suhir, E. Connally, and D. Steinberg (Springer 20111)

[5] Ghaffarian, R., "Area Array Technology for High Reliability Applications," Chapter 16 in *Micro-and Opto-Electronic Materials and Structures: Physics, Mechanics, Design, Reliability, Packaging*, ed. E. Suhir (Springer, 2006).

[6] Ghaffarian, R. "CCGA Packages for Space Applications," *Microelectronics Reliability* 46 (2006) 2006–2024.

[7] Ghaffarian, R., "BGA Assembly Reliability," Chapter 20 in *Area Array Packaging Handbook*, ed. K. Gilleo (McGraw-Hill, 2004).

[8] Fjelstad, J., Ghaffarian, R., and Kim, Y.G., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002).

[9] Licari, J.J., Swanson, D.W., *Adhesives Technology for Electronic Applications, Materials, Processing*, Reliability, 2nd Edition, June 23, 2011, Elsevier

[10] Ghaffarian, R., "Reliability of PWB Microvia for High Density Package Assembly," *International Journal of Materials and Structural Integrity*, 2008, Vol. 2, No. 1–2, pp. 47–63.

[11] Ojeda, C.E., Oakes, E.J., Hill. J.R., Aldi, D., Forsberg, G.A, "Temperature Effects on Adhesive Bond Strengths and modulus for commonly used spacecraft structural Adhesives," Jet Propulsion Laboratory,
trs-new.jpl.nasa.gov/dspace/bitstream/2014/42025/1/11-0955.pdf

[12] Popelar, S.F., "A Parametric Study of Flip Chip Reliability Based on Solder Fatigue Modeling," *IEEE/CPMT Int'l Electronics Manufacturing Technology Symposium*, 1997.

[13] Kwak, J.B., Chung, S., "The effects of Underfill on the Thermal Fatigue Reliability of Solder Joints in Newly Developed Flip Chip on Module," *IEEE InterSociety Thermal Conference (ITherm)*, San Diego, CA May 31–June 2, 2012.

[14] Robers, J., Hussain, S., Suhling, J., Jaeger, R., Lall, P., "Characterization of Die Stresses in Microprocessor Packages Subjected to Thermal Cycling," *IEEE InterSociety Thermal Conference (ITherm)*, San Diego, CA May 31–June 2, 2012.

[15] Quinones, H., "Capillary Underfill Physical Limitations for Future Package," www.ipcoutlook.org/pdf/**capillary**_underfill_future_packages_**smt**a.pdf.

[16] Agarwal, S., et al., " Class Y: A New QML Class for Non-Hermetic Space Products," *3rd NASA Electronic Workshop (ETW)*, June 2012.

[17] Bolger, J.C., Mooney, C.T., "Die Attach in Hi-Rel P-DIPs: Polyimides or Low Chloride Epoxies." *IEEE Transaction Component Hybrids Manufacturing Technology*, Vol. CHMT-7, No.4, pp.394–398, 1984.

[18] Engelmaier, W., "Solder Joint Reliability, Accelerated Testing and Result Evaluation," chapter in *Solder Joint Reliability: Theory and Applications*, John Lau, ed., Van Nostrand Reinhold, New York, 1990.

[19] Peng, H., Johnson, R.W., Flowers, G., Ricketts, A.,Yeager, E., Konarski, M., "Underfilling Fine Pitch BGAs," *IEEE Transactions on Packaging Manufacturing*, October 2001.

[20] Tian, G., Liu, Y., Johnson, W., Lall, P., Palmer, M., Islam, M., Crane, L., Yeager, E., Konarski, M., Torres, A., "Corner Bonding of CSPs: Processing and Reliability," *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 28, No.3, July 2005, 231.

[21] Shi, B.H., Ueda, T., "Mitigation of Thermal Fatigue Failure in Fully Underfilled Lead-free Array-based Package Assemblies Using Partial Underfills," *Proceeding of 13th Electronics Packaging Technology Conference*, 2011

[22] Mawer, A., Koschmieder, T., Galles, P., "Assembly and Reliability of Preform Underfilmed BGAs in Drop Test and Thermal Cycling," *Proceedings of Surface Mount Technology*, 2011

[23] Burnette, T., Johnson, Z., Koschmieder ,T., Oyler, W., "Underfilled BGAs for Ceramic BGA Packages and Board-Level Reliability," *IEEE Electronic Components and Technology Conference*, 2000.

[24] Ghaffarian, R., "Thermal Cycle Reliability and Failure Mechanisms of CCGA and PBGA Assemblies with and without Corner Staking," *IEEE Transactions on Components and Packaging Technologies*, June 2008, Vol. 31, Issue 2.

[25] Chan, Y., Song, F., Lee. S.W., "Investigation on Lead-free Solder Joint Reliability of Edge-bonded CBGA Under Temperature Cycling," *2011 International Conference on Electronic Packaging Technology and High Density Packaging.*