ATJ2259B Datasheet

Latest Version: 1.1

2009-10-27

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3 *Revision History*

Date	Revision	Description
2009-10-12	1.0	New Release
2009-10-27	1.1	1. Functional Block modified; 2. Notes added to 17.3.4. 3. 25.3.7 GPIO_MFCTL2 & 25.3.8 PAD_DRV added; 4. 28.16.2 LDR LCM Driver Parameter added.

4 Introduction

4.1 Overview

ATJ2259B is highly integrated 32bit RISC-based SOC for media solution. The RISC architecture and high speed bus controller can achieve high performance and low power dissipation. With a built-in media coprocessor, its media platform can deal with MJPEG, MPEG4, H263, H264 and WMV format more efficiently. A USB v2.0 (HS) SIE with OTG function was integrated, making the platform act as a host or slave mass storage device at the speed up to 480Mbps. The audio codec in the SOC is based on delta-sigma modulation, which can get high performance with low power and allow the flexible adjustment of sample rate from 8k to 96k. The built-in audio codec can switch inputs within headphones, microphone and FM radio and direct drive the low impedance earphone. ATJ2259B also provides TVOUT for PAL/NTSC CODEC, easily converting video signal between analog and digital. For various memories, the SOC integrates SRAM, SDRAM, FLASH, SD/MMC, MS etc. The platform also offers I2C, SPI, UART, IR and SPDIF interfaces for changeful control and transfer modes. Thus, ATJ2259B provides a true "ALL-IN-ONE" solution that is ideally suited for highly optimized digital media devices.

4.2 Features

	ATJ2259B
Package	LQFP176（20mmX20mm）
SDRAM	16bit
Memory	Nand, SD/MMC and MS
Display	TVOUT/CPU interface LCM/RGB interface LCM
Extension Interface	I2C/UART/IR/SPI/SPDIF
Key-press	4X3P/4X16S/remote
USB	OTG/host/slave
CMOS Sensor	Built-in
TV IN	Supported
TP	Built-in

32BIT RISC CORE

- 8-stage pipeline MIPS24Kecp core
- Software can program from DC up to 288MHz transparently
- SIMD DSPASE for audio and so on Application Specific
- 16kB Dcache + 16KB Icache
- 24kB DSPRAM（Data ScratchPad RAMs）
- 8kB ISPRAM（Instruction ScratchPad RAMs）
- Standard Memory Management Unit, 32 dual-entry JTLB with variable page sizes
- High performance Actions media UDI（User Defined Instruction）

24BIT DSP CORE

- 24 bits instructions and data bus
- 1 instruction per Machine Cycle
- Software can program from DC up to 90MIPS

CLOCK

- Build-in low frequency oscillator, about 32KHz
- LOSC:32.576KHz 20 ppm for DRM
- HOSC:24MHz 30ppm for TVOUT
- RTC (Real Time Clock),surport DRM9, DRM10
- 2-channel CTC (Counter/Timer Controller) and watch dog circuit

AUDIO CODEC

- Build-in Stereo 18-bit Sigma-Delta DAC: SNR>88db (no a-weight), 18bits,sample rate 8/11.025/12/16/22.05/24/32/44.1/48/96
- Support FM Radio input and 32 levels volume control
- Stereo 21-bit Sigma-Delta ADC for Microphone/FM Input: SNR >80dB, sample rate 8/11.025/12/16/22.05/24/32/44.1/48/96,solution:18bit
- IIS Input or output support 96k sample rate
- Headphone driver output 2x18mW @16 Ohm

Local MEMORY

- RAM on chip (32k*24bit)
- ROM on chip (38k*32bit)
- OTP ROM 128bit Chip ID

SDRAM

- Compatible to JEDEC standard
- SDR SDRAM and Mobile SDR SDRAM are supported

- up to 512MbX16 with speed up to 200Mbytes/s
- Supports Auto Refresh mode, Self Refresh mode and power-down mode
- Supports all power-saving features (PASR, TCSR & Deep Power Down) for Mobile SDRAM
- Programmable timing parameters. tWR, tWTR, tRCD, tRP, tMRD, tRFC, tXP, tXSR/tXSNR, tRFC
- Auto Low Power Management

NAND

- up to 8k page size
- support 4 CE,2 RB nand flash
- support 1bit hamming ECC and 8bits/12bits BCH ECC
- SLC & MLC NAND Flash support
- also suport SMD, XD, LBA nand

SD/MMC

- Compatible to MMC card specification 4.2
- compatible to SD memory card physical layer specification version 2.00
- Support SDIO function
- Support SD/HCSD/microSD/miniSD memory card, MMC/RSMMC/MMCPLUS card, INAND, MOVINAND, eMMC,CE-ATA Micro Drive,SDIO card etc.
- Support 1 bit,4bit,8bit bus mode
- clock max rate up to 52MHz
- Read /Write CRC Status Hardware auto checked
- Support Auto Block mode

MS

- Compatibility with Memory stick stand format specification ver1.43
- Compatibility with Memory stick PRO format specification ver1.02
- Compatibility with Memory Stick Micro Format specification ver1.01
- Compatibility with Memory Stick Pro-HG Card Format Specification Ver1.01
- Support MS STD,MS DUO,MS PRO,MS PRO DUO,MS,MS HG.
- Maximum Capacity: MS card-128MB,MS pro/micro-32GB
- Support 1 bit,4bit bus mode
- Maximum transmission clock: serial-20MHz; parallel-40MHz

USB

- Complies with On-The-Go Supplement to the USB2.0 Specification Revision 1.0a
- UTMI+ level2 Transceiver Macrocell Interface
- Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)

- upports point-to-point communication with one low-speed, full-speed or high-speed device in Host mode (no HUB support)
- Supports full-speed or high-speed in peripheral mode
- Supports high-speed high-bandwidth Isochronous and Interrupt transfer
- Supports suspend, resume and power management function.Support remote wakeup
- Support USB 2.0 Compliance PHY+SIE, 60MBps

TV IN

- Support ITU-R BT601/BT656 input data format
- Support selectable reception for field, line and point（1:1/2:1/4:1）
- Vsync, Hsync and Field's polarity is adjustable
- Compatible with mainstream decoder on the market.

TV OUT

- ITU-R BT601/BT656 YCrCb to PAL/NTSC video encoder
- Support NTSC-M,-J and –4.43 mode
- Support PAL-B, -D, -G, -H, -I, -M, -N, -Nc mode
- CVBS (Composite Video Broadcasting Signal) output
- High quality 10-bit video DACs
- Programmable default output color
- 32-bit direct digital synthesizer for color sub-carrier
- Programmable color-burst phase and line sync amplitude
- Programmable contrast/brightness/saturation
- Complete on-chip video timing generator
- On-board color bar generation

I2C

- Complies with I2C Bus Specification V2.1
- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Multi-slave capability
- Hi-speed mode and 10bit address mode not supported
- Internal Pull-Up Resistor (2.7k) optional

UART

- 2 UART: UART1 and UART2
- Capable of speeds up to 1.5Mbps to enable connections with Bluetooth and other peripherals
- Baud rate is changeable

- 5-8 Data Bits and LSB first in Transmit and Received, and 1-2 Stop Bits
- Support Even, Odd, or No Parity
- UART1 support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system

IR

- Complies with IrDA Physical Layer Specification V1.4
- Support SIR, MIR and FIR mode
- SIR speed range from 2400 to 115200 bps with pulse width 3/16 bit mode; and speed range from 9600 to 115200 bps with pulse width 1.6us mode
- Speeds 0.576 and 1.152 Mbps for MIR mode and 4Mbps for FIR mode, with 1/4 mark-to-space ratio

SPI

- Support master mode and slave mode. The speed of master mode up to 50Mbps, and slaver up to 10Mbps
- Support SPI four standard mode, mode 0\1\2\3
- Two wire mode capability, only use SCLK and MOSI signal

SPDIF

- Support sample rate 32k\44.1k\48k
- Partly complies with IEC958
- Support SPDIF in and out

LDC (CPU Interface LCD)

- Support 8080 interface LCD panels
- Support multi format display: 16bit (RGB 565 1transfer); 18bit (RGB 666 1transfer); 8bit (RGB 565 2transfer); 9bit (RGB 666 2transfer); 8bit (RGB 888 3transfer) ;6bit (RGB 666 3transfer)
- RGB and BGR is configurable
- build-in PWM singnal

LDR (RGB Interface LCD)

- Support parallel and serial RGB interface LCD panels
- Support multi format display: 18-bit parallel; 16-bit (5-6-5 format) parallel; 24-bit (8-8-8 format) serial;18-bit (6-6-6 format) serial
- RGB, RBG, GRB , GBR , BRG and BGR is configurable
- Support programmable synch signals timing, and adaptive to various LCD panels
- build-in PWM singnal

CMOS Sensor

- 8 bit YCbCr/RGB565 format image input
- Input image sub-sample function
- Vsync, Hsync and PCLK's polarity is adjustable
- With CLKTOUT for CMOS Sensor 's External CLK (up to 60Mhz)

TP

- Build in 4 wire resistance touch panel controller
- ADC's resolution is 11-bit
- Auto (Sequential) X/Y Position Conversion Mode
- Stylus up/down detect automatically
- Programmable sensitivity setting

KEY

- Parallel mode and serial mode hardware scanner
- The max scan matrix is 4×3 in parallel mode and 4×16 in serial mode
- Hardware de-bounces
- Programmable sensitivity setting
- Supports multiple key presses for gaming

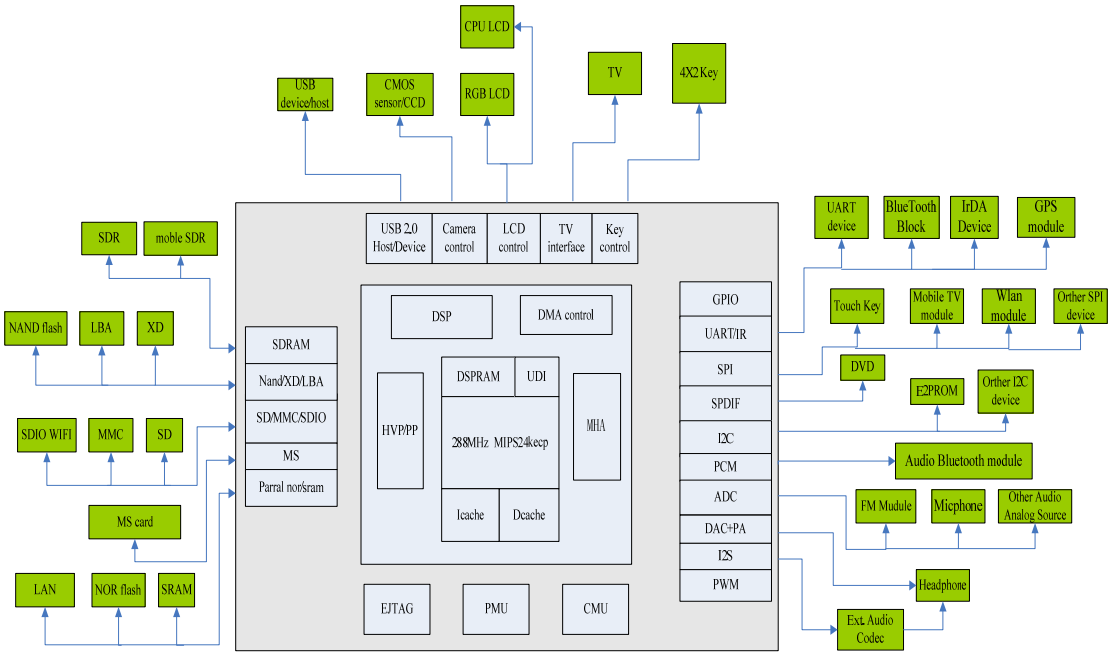
LOW POWER

- Support low power standby mode and can be woke up by 5 recover trig source
- Energy saving dynamic power management (PMU), supporting standard Li-ion bat, with constant current and constant voltage charger

FORMAT SUPPORT

- WAV, MP1, MP2, ASF, WMA, FLAG, OGG, APE, AUDIBLE
- JPEG, BMP, TIF
- MJPEG,XVID, WMV, H264, H264,FLV, 3GP, SWF

5 *Functional Block*



6 PMU/DC-DC Converter

6.1 Description

ATJ2259B PMU include:

- DC/DC (VDD) Converters work in buck mode. The output voltage is 1.6V, programmable;
- Two regulators, whose output voltages are 3.1V and 1.6V, programmable;
- A bias current generator.
- 6 bits low speed ADC, whose input range is from 0.7V to 1.5V, monitors batteries voltage.
- 6bits low speed ADC, whose input range is from 0V to 3.1V, monitors remote control signal.
- Battery charger, support Li+ battery.

6.2 Registers List

CMU Block Base Address

Module name	Physical Bass Address	KSEG1 Base Adress
PMU	0x10000000	0xB0000000

Configuration Registers Offset

Offset	Register Name	Description
0x00	PMU_CTL	PMU Control Register
0x04	PMU_LRADC	PMU Low Resolustion ADC Register
0x08	PMU_CHG	PMU Charg Control Register

6.3 Registers Description

6.3.1 PMU_CTL

DC/DC Converter and Regulator's register

Offset=0x0000

Bits	Name	Descriptions	R/W	Reset
31	LBRM	Low Battery Reset Mask bit LB_ mask, "1",OPEN	R/W	1
30..28	VCVS	VCC Voltage Set Register 3.3V* 111 3.2V 110 3.1V 101 3.0V 100 2.9V 011 2.8V 010 2.7V 001 2.6V 000	R/W	0x7
27	LBNM	Low Battery Nom-Masked Interrupt Mask bit LBNMI_ mask, "1", OPEN	R/W	1
26..24	VDVS[3:1]	VDD Voltage Set Register 2.0V 111 1.9V 110 1.8V* 101 1.7V 100 1.6V 011 1.5V 010 1.4V 001 1.3V 000	R/W	0x5
23:15	—	Reserved	R/W	xCE
14	VCOE	VCCOUT Enable 1:Enable 0:Disable	R/W	1
13	BATADC	BATADC Enable 1:Enable 0:Disable	R/W	0
12	REMADC	REMADC Enable 1:Enable	R/W	0

		0:Disable		
11-10	IBIAS	Current bias control 00:0.92uA 01:0.96uA 10:1.0uA 11:1.04uA	R/W	0x2
9-8	OSCFREQ	PMU Oscilator Frequency Set Freq. Current 00 470KHz 1.5uA 01 600kHz 2.0uA 10 750kHz 2.5uA 11 880kHz 3.0uA	R/W	0x1
7	DC1M	DCDC1 Mode 1:PWM 0:PFM	R/W	1
6:3	-	Reserved	R	0xD
2	VDV0	VDD Voltage Set bit0 1: +50mV for VDD	R/W	0
1-0	-	Reserved	R	0x3

6.3.2 PMU_LRADC

Low Resolution ADC Data Register

Offset=0x0004

Bits	Name	Descriptions	R/W	Reset
31	DC5V	DC5V availbe for charge. 1:available 0:unavailable	R	0
30	RemADC_Average	RemADC Average slect 0—— no avergae 1—— 2 times average	R/W	1
29-28	RemADCSample	Remote ADC sample frequency select 00——64Hz 01——128Hz 10——256Hz 11——512Hz	R/W	01

27-22	REMOADC6	Remote Control 6bit Voltage ADC Range:0-AVCC	R	x
21-16	BATADC6	Battery 6bit Voltage ADC Range: 1A:0.7-1.5V 2A:1.4-3.0V Li+:2.1-4.5V	R	x
15-0	—	Reserved	R	0

6.3.3 PMU_CHG

PMU Charger Control and Status register

Offset=0x0008

Bits	Name	Descriptions	R/W	Reset
31	EN	Enable Charge Circuit 1: Enable charge circuit 0: Disable charge circuit. Charge circuit will not work and consume little power.	R/W	0
30-28	CURRENT	Charge Current Configure 000:50mA 001:100mA 010:150mA 011:200mA 100:250mA 101*:300mA 110:400mA 111:500mA	R/W	0x5
27	STAT	Charging Status. 0: not charging, 1: charging.	R	0
26-25	CHGPHASE	Charging phase 00 Reserved 01 Pre-charging 10 Constant current 11 Constant voltage The two bits will be available	R	00

		Only when bit 31 of this register is set, or will be always read 00.		
24	—	Reserved	R/W	0x1
23	CHTE	Charger test	R/W	0
22-16	-	Reserved	R/W	0x5
15	PBLS	PWM BL_NDR able 0: disable 1: enble PWM pulse output	R/W	0
14	PPHS	PWM SELECT,this bit in effect only when PBLS is 1 0: LOW IS SELECT 1: HIGH IS SELECT	R/W	0
13	-	Reserved	R/W	0
12-8	PDUT	PWM Back Light Duty 00000 0/32 00001 1/32 00010 2/32 . 11110 30/32 11111 31/32	R/W	01111
7-4	-	Reserved	R/W	1
3-2	LBNMIVS	Low Battery Non-mask Interrupt Voltage Setting Li+ 00* 2.9V 01 3.1V 10 3.3V 11 3.5V	R/W	0
1-0	LBRVS	Low Battery Reset Voltage setting Li+ 00 2.7V 01 2.9V 10 3.1V 11 3.3V	R/W	1

7 CMU/HOSC, RTC/LOSC/Watch Dog, Time Count

7.1.1 CMU/HOSC Register List

Base Address

Block Name	Physical Base Address	KSEG1 Base Address
CMU	0x10010000	0xB0010000

HOSC/CMU Regiser Address

REG Name	Offset	Description
CMU_UART1CLK	0x0028	Uart1 Clk Control Register
CMU_UART2CLK	0x002C	Uart2 Clk Control Register
CMU_FMCLK	0x0034	FM Clk Control Register
CMU_DEVCLKEN	0x0080	Device Clk Enable Control Register
CMU_DEVRST	0x0084	Device Reset Control Register

7.1.2 CMU/HOSC Register Description

7.1.2.1 CMU_UARTxCLK

Uart1 Clk Control Register

Offset=0x0028

Uart2 Clk Control Register

Offset=0x002C

Bits	Name	Description	R/W	Reset
31..17	-	Reserved	R	0
16	UxEN	Uartx Clock Enable 1:Enable 0:Disable	Rw	0
15..0	UARTxDIV	Uartx Clock Divisor Uartx_CLK=C_CLKlk/(UARTxDIV +1)	Rw	0

7.1.2.2 CMU_FMCLK

FM Clk Control Register

Offset= 0x0034

Bits	Name	Description	R/W	Reset
31..6	-	Reserved	R	0
5	BCKE	PWM Back Light clock Enable 0:disable 1:enable	RW	0
4	BCKS	Back Light CLK source select 0:LOSC 32k 1:HOSC/8 3M	RW	0
3:2	BCKCON	Divided PWM Back Light Special Clock Control LOSC HOSC/8 00: 32k 3M 01: 16k 1.5M 10: 8k 750k 11: 4k 375k	RW	0
1	CLKS	FM Clock Output Selection 0:32.768k 1:24M	RW	00
0	OUTE	FM Clock Output Enable(From Test Pin) 1:Enable test pin output Clock 0:Disable test pin output	RW	00

Note: Test pin can be configed to output osilator clock 32k or 24M. When OUTE is set 0, test pin has the “test” function. When set 1, and test pin has the clock out function.

7.1.2.3 CMU_DEVCLKEN

Device Clk Control Register

Offset=0x0080

Bits	Name	Description	R/W	Reset
31..27	-	Reserved	R	0
26	GPIO	GPIO control reg clock enable. Switch APB clock	RW	0
25	Key	KEY control reg clock enable. Switch APB clock.	RW	0
24	SPI	SPI control reg clock enable. Switch APB clock.	RW	0
23	IIC	IIC control reg clock enable.	RW	0

		Switch APB clock.		
22	UART	UART control reg clock enable. Switch APB clock and UART special clock.	RW	0
20	SPDF	SPDIF control reg clock enable. Switch APB clock and Audio special clk.	RW	0
19:0	-	Reserved	RW	0

7.1.2.4 CMU_DEVRST

Device Reset Control Register

Offset＝0x0084

Bits	Name	Description	R/W	Reset
31	-	Reserved	RW	1
30	GPIO	GPIO control Block reset	RW	1
29	Key	KEY control Block reset.	RW	1
28	-	Reserved	RW	1
27	IIC	IIC control Block reset.	RW	1
26	UART	UART control Block reset.	RW	1
24	SPDF	SPDIF control reg Block reset.	RW	1
23-11	-	Reserved	RW	0x1fff
10	SPI	SPI Block reset.	RW	1
9-0	-	Reserved	RW	0x3ff

Note: Write '0' to reset the block

7.2 RTC/LOSC/Watch Dog, Timer 0, 1

7.2.1 Description

RTC has 5 individual units: 2Hz, Calendar, Alarm, WD, Timer0/1. Each module is simply operated.

7.2.1.1 2HZ

2Hz IRQ will generate every 0.5 second if enable 2HZ. It can be cleared by writing 1 to the bit 2HIP.

7.2.1.2 Calendar

When RTCE=1, ***RTC_DHMS*** and ***RTC_YMD*** count up with LOSC_CLK1. MCU can read the

two registers at any time for getting the real time, but can not write the two registers. When RTCE=0, the two registers can be written to set the real time.

7.2.1.3 Alarm

When RTCE=ALIE=1, if ***RTC_DHMSALM=RTC_DHMS*** and ***RTC_YMDALM=RTC_YMD***, Alarm IRQ will generate, It can be cleared by writing 1 to the bit ALIP.

7.2.1.4 Watch Dog

Write 1 to WDEN will enable WD. when WD timer overflows, An internal reset or IRQ is generated. An internal reset is generated to force the system into reset status and then reboot.The WD timer overflows interval is set by CLKSEL.

Write 1 to CLR will clear the WD timer. The CLR will be cleared automatically after the WD timer cleared

Write 1 to IRQP will clear the WD IRQ pending.

7.2.1.5 TIMER0/1

When EN=1, ***RTC_T0*** count down until equal to zero, If ZIEN=1, An IRQ will generate when ***RTC_T0***=0. The IRQ can be cleared by writing 1 to ZIPD.

When EN=0, ***RTC_T0*** can be written, but timer0 do not work.

7.2.2 LOSC/RTC/Watch Dog Register List

Base Address

Name	Physical Base Address	KSEG1 Base Address
RTC	0x10018000	0xB0018000

HOSC/CMU Regiser address

Control Reg Name	Offset Address	Description
RTC_CTL	0x0000	RTC Control Register
RTC_DHMS	0x0004	RTC Day Hour Minute and Second Register
RTC_YMD	0x0008	RTC Year Month Date Register
RTC_DHMSALM	0x000C	RTC Day Hour Minute and Second Alarm Register
RTC_YMDALM	0x0010	RTC Year Month Date Alarm Register
RTC_WDCTL	0x0014	RTC Watch Dog Control register
RTC_T0CTL	0x0018	RTC Timer0 Control register
RTC_T0	0x001C	RTC Timer0 Value
RTC_T1CTL	0x0020	RTC Timer1 Control register
RTC_T1	0x0024	RTC Timer1 Value

NOTE1: When reading Register DAY_HOUR_MIN_SEC, YEAR_MON_DATE YEAR_MON_DATE,

program can get the real value, until reading the same value in continuous three times.
NOTE2: When Seting the RTC, WD, COUNT0/1, program must disable the conresponding enable bit at first and then enable it after seting the value.

7.2.3 RTC/LOSC/Watch Dog Register Description

7.2.3.1 RTC_CTL

RTC Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31..12	-	Reserved	R	0
11	RST	RTC Reset 1:Normal 0:Reset	RW	1
10	-	Reserved	RW	0
9	LEAP	RTC Leap Year bit 1:leap year 0:non leap year	R	1
8-7	-	Reserved	R	1
6	EOSC	External Crystal OSC enable, 0: Disable, 1: Enable	RW	1
5	CKSS1	Low Frequence Clock Source Select, 0: Build-in OSC (about 32K), 1:External Crystal OSC	RW	0
4	RTCE	RTC Enable, 0: Disable, 1: Enable	RW	1
3	2HIE	2Hz IRQ Enable 0: Disable, 1: Enable	RW	0
2	ALIE	Alarm Irq Enable, 0:Disable, 1:Enable (POR- RESET)	RW	0
1	2HIP	2Hz IRQ Pending bit, writing 1 to this bit will clear it	RW	0
0	ALIP	Alarm IRQ Pending bit(POR- RESET),writing 1 to this bit will clear it	RW	0

Note:

1. Changeing RTC register must set RTCE to"0"first and then set it back to "1".
Alarm Irq can wake the system.
2. Bit5:CKSS1 will be reset only when RTCVDD is power off.

7.2.3.2 RTC_DHMS

RTC Day Hour Minute and Second Register
Offset=0x0004

Bits	Name	Description Binary code	R/W	Reset
31..27	-	Reserved	R	0
26..24	DAY	01H-07H	RW	-
23..21	-	Reserved	R	0
20..16	HOUR	00H-17H	RW	-
15..14	-	Reserved	R	0
13..8	MIN	00H-3BH	RW	-
7..6	-	Reserved	R	0
5..0	SEC	00H-3BH	RW	-

Note: This register reset by RST bit in RTC_Con Register.

7.2.3.3 RTC_YMD

RTC Year Month Date Register
Offset=0x0008

Bits	Name	Description Binary code	R/W	Reset
31	-	Reserved	R	0
30..24	CENT	00H-63H	RW	-
23	-	Reserved	R	0
22..16	YEAR	00H-63H	RW	-
15..12	-	Reserved	R	0
11..8	MON	01H-0CH	RW	-
7..5	-	Reserved	R	0
4..0	DATE	01H-1FH	RW	-

Note: It can detect the leap year and month.
This register reset by RST bit in RTC_Con Register.

7.2.3.4 RTC_DHMSALM

RTC Day Hour Minute and Second Alarm Register

Offset=0x000C

Bits	Name	Description Binary code	R/W	Reset
31..21	-	Reserved	R	0
20..16	HOURAL	00H-17H	RW	0x1f
15..14	-	Reserved	R	0
13..8	MINAL	00H-3BH	RW	0x3f
7..6	-	Reserved	R	0
5..0	SECAL	00H-3BH	RW	0x3f

7.2.3.5 RTC_YMDALM

RTC Year Month Date Alarm Register

Offset=0x0010

Bits	Name	Description Binary code	R/W	Reset
31..23	-	Reserved	R	0x9d
22..16	YEARAL	00H-63H	RW	0x7f
15..12	-	Reserved	R	0
11..8	MONAL	01H-0CH	RW	0xe
7..5	-	Reserved	R	0
4..0	DATEAL	01H-1FH	RW	0x1e

7.2.3.6 RTC_WDCTL

RTC Watch Dog Control registers

Offset=0x0014

Bits	Name	Description	R/W	Reset
31..7	-	Reserved	RW	0
6	IRQP	Watch dog IRQ pending bit,writing 1 to this bit will clear it	RW	0
5	SIGS	Watchdog Signal (IRQ or Reset-) Select.0: Irq, 1: Reset-. 1: Send Reset signal when watchdog overflow. 0: Send IRQ signal when watchdog overflow.	Rw	0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is	Rw	0

		generated to force the system into reset status and then reboot		
3..1	CLKSEL	Watch Dog timer Clock Select, WDCKS Clock Selected Watch Dog Length 000 1 KHz 176 ms 001 512 Hz 352 ms 010 128 Hz 1.4 s 011 32 Hz 5.6 s 100 8 Hz 22.2 s 101 4 Hz 45 s 110 2 Hz 90 s 111 1 Hz 180 s	Rw	0
0	CLR	Clear bit, write 1 to clear WD timer, cleared automatically	RW	0

7.2.3.7 RTC_T0CTL

RTC Timer0 Control register

Offset=0x0018

Bits	Name	Description	R/W	Reset
31..6	-	Reserved	R	0
5	EN	Timer 0 Enable 0:Disable,1:Enable	RW	0
4..3	-	Reserved	R	0
2	RELO	Timer 0 Reload. 0:Not reload,1:Reload	RW	0
1	ZIEN	T0 Zero IRQ Enable When this bit is enabled, TIMER0_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer0 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The Count only can count down. When count becomes zero, IRQ will be sent.

7.2.3.8 RTC_T0

RTC Timer0 value register

Offset=0x001C

Bits	Name	Description	R/W	Reset
31..24		Reserved	R	0
23..0	T0	Read or write current Timer0 value	RW	-

7.2.3.9 RTC_T1CTL

RTC Timer1 Control register

Offset=0x0020

Bits	Name	Description	R/W	Reset
31..6	-	Reserved	R	0
5	En	Timer0 Enable 0:Disable,1:Enable	RW	0
4..3	-	Reserved	R	0
2	RELO	Timer1 Reload 0:Not reload,1:Reload	RW	0
1	ZIEN	Timer1 Zero IRQ Enable When this bit is enabled, TIMER1_Zero_IRQ sent out the irq signal until the pending bit was cleared.	RW	0
0	ZIPD	Timer1 IRQ Pending, Writing 1 to clear this bit.	RW	0

Note: The Count only can count down. When count becomes zero, IRQ will be sent.

7.2.3.10 RTC_T1

RTC Timer1 Value

Offset=0x0024

Bits	Name	Description	R/W	Reset
31..24		Reserved		
23..0	T1	Read or write current Timer1 value	RW	0

8 *Interrupt Controller*

8.1 Descriptions

8.1.1 Summary

The interrupt controller supports 32 interrupt sources. It can generate five outputs as interrupt requests 0, 1, 2, 3 and 4. Each of these outputs are connected to the CPU core.

8.1.2 Interrupt Sources

Note: Details about the interrupt sources can be found in the respective peripheral sections.

Table Interrupt Sources

Interrupt Number	Sources	Type
0-7	Reserved	High Level
8	2Hz/WatchDog	High Level
9	TIMER1	High Level
10	TIMER0	High Level
11	RTC	High Level
12	Reserved	High Level
13	Key	High Level
14	External	High Level
15	TP	High Level
16	SPI	High Level
17	IIC2	High Level
18	IIC1	High Level
19	UART2	High Level
20	UART1	High Level
21-22	Reserved	High Level
23	SPDIF	High Level
24	Reserved	High Level
25	PCM	High Level

26-31	Reserved	High Level

8.1.3 External Interrupt Sources

The interrupt controller has two external interrupt sources, which input from SIRQ0/1. They can be configed as level or edge-triggered interrupt. When using external interrupt source, corresponding multi function pad must be set input mode.

8.2 Interrupt Controller Registers Lists

TableBase Address

Name	Physical Base Address	KSEG1 Base Address
INTC	0x10020000	0xB0020000

Table INTC Regiser address

Register Name	Offset	Description
INTC_PD	0x0000	Interrupt Pending register
INTC_MSK	0x0004	Interrupt Mask register
INTC_CFG0	0x0008	Interrupt Config register 0
INTC_CFG1	0x000C	Interrupt Config register 1
INTC_CFG2	0x0010	Interrupt Config register 2
INTC_EXTCTL	0x0014	External Interrupt control and status register

8.3 Interrupt Controller Registers Description

8.3.1 INTC_PD

Interrupt Pending Register.

CPU can access the status of interrupt sources by read this register.

Offset=0x0000

Bits	Name	Description	Read/Write	Reset
31:0	INTC_PD[n]	Interrupt Pending bit.Interrupt nume “n” accords to **Interrupt Sources Table**. 0:Interrupt source n request is not active	R	0

		1: Interrupt source n request is active.		

8.3.2 INTC_MSK

Interrupt MASK Register.

CPU can enable or disable by write this register.

Offset=0x0004

Interrupt Mask.

0: Interrupt is disabled.

1: Interrupt is enabled.

Bits	Name	Description	R/W	Reset
31..26	-	Reserved	RW	0
25	PCM	PCM Interfae Interrupt Mask Bit	RW	0
24	-	Reserved	RW	0
23	SPDF	SPDIF Interface Interrupt Mask Bit	RW	0
22-21		Reserved	RW	0
20	URT1	URT1 Interrupt Mask Bit	RW	0
19	URT2	URT2 Interrupt Mask Bit	RW	0
18	IIC1	IIC1 Interrupt Mask Bit	RW	0
17	IIC2	IIC2 Interrupt Mask Bit	RW	0
16	SPI	SPI Interrupt Mask Bit	RW	0
15	-	Reserved	RW	0
14	EXT	External IRQ Interface Interrupt Mask Bit	RW	0
13	KEY	KEY Interrupt Mask Bit	RW	0
12	-	Reserved	RW	0
11	RTC	RTC Interrupt Mask Bit	RW	0
10	T0	T0 Interrupt Mask Bit	RW	0
9	T1	T1 Interrupt Mask Bit	RW	0
8	WD	WatchDog Interrupt Mask Bit	RW	0
7-0	-	Reserved	RW	0

8.3.3 INTC_CFGx

Interrupt Config Registers. CPU can assign anyone interrupt source to one of the five interrupt requests.

INTC_CFG0:

Offset=0x0008

INTC_CFG1:

Offset=0x000C

INTC_CFG2:

Offset=0x0010

INTC_CFG2[n]	0	0	0	0	1
INTC_CFG1[n]	0	0	1	1	x
INTC_CFG0[n]	0	1	0	1	x
The interrupt request be assigned	0	1	2	3	4

Bits	Name	Description	R/W	Reset
31..26	-	Reserved	RW	0
25	PCM	PCM Interfae Interrupt CFGx Bit	RW	0
24	-	Reserved	RW	0
23	SPDF	SPDIF Interface Interrupt CFGx Bit	RW	0
22-21		Reserved	RW	0
20	URT1	URT1 Interrupt CFGx Bit	RW	0
19	URT2	URT2 Interrupt CFGx Bit	RW	0
18	IIC1	IIC1 Interrupt CFGx Bit	RW	0
17	IIC2	IIC2 Interrupt CFGx Bit	RW	0
16	SPI	SPI Interrupt CFGx Bit	RW	0
15	-	Reserved	RW	0
14	EXT	External IRQ Interface Interrupt CFGx Bit	RW	0
13	KEY	KEY Interrupt CFGx Bit	RW	0
12	-	Reserved	RW	0
11	RTC	RTC Interrupt CFGx Bit	RW	0
10	T0	T0 Interrupt CFGx Bit	RW	0
9	T1	T1 Interrupt CFGx Bit	RW	0
8	WD	WatchDog Interrupt CFGx Bit	RW	0
7	PCNT	Performance Count Interrupt CFGx Bit	RW	0
6-0	-	Reserved	RW	0

8.3.4 INTC_EXTCTL

External Interrupt Control and Status register. When one of the external interrupt arrises, the corresponding pending bit of INTC_PD will be set.

Offset=0x0014

Bits	Name	Description	Read/Write	Reset
31:27	-	Reserve.	R	0
26:25	E1TYPE	External Interrupt 1 Type 00 High level active. 01 Low level active. 10 Rising edge-triggered. 11 Falling edge-triggered.	RW	00
24	E1EN	Enable External interrupt 1(irq) 0 Disable 1 Enable	RW	0
23:17	-	Reserve.	R	0
16	E1PD	External Interrupt 1 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 1 is edge-triggered, this bit must be cleared by software after detected.	R/W	-
15:11	-	Reserve.	R	0
10:9	E0TYPE	External interrupt 0 type 00 High level active. 01 Low level active. 10 rising edge-triggered. 11 Falling edge-triggered.	R/W	0
8	E0EN	Enable external interrupt 0(irq) 0 Disable 1 Enable	R/W	0
7:1	-	Reserve.	R	0
0	E0PD	External Interrupt 0 Pending 0 External interrupt source 0 is not active. 1 External interrupt source 0 is active. Write 1 to the bit will clear it. If external interrupt source 0 is edge-triggered, this bit must be cleared by software after detected.	R/W	0

9 32bit Mips24KEc Core

ATJ2259B processor core (Mips24KEc) is an excellent implementation of MIPS32™ Release 2 instruction set architecture designed for high performance and low power. The core includes the following main components:

- Instruction pipeline with multiply/divide unit (MAC) and register file
- Coprocessor 0 registers (System Control Coprocessor)
- Instruction and data caches
- Programmable Memory Management Unit (translation-lookaside buffer)
- AHB bus interface

10 *DMA*

ATJ2259B DMA controller contains 8 tasks, which are divided into two types, bus DMA and special channel DMA. System bus adopts the subset of AMBA bus protocol.

11 *SDRAM Interface*

11.1 General Description

SDRAM interface controller provides a high performance interface to single data rate (SDR) synchronous dynamic random access memory (SDRAM) devices. The controller accepts read and write commands using the asynchronous FIFO from host, and translates these requests to the command sequences required by SDR devices. The controller also performs all initialization and refresh functions.

The controller uses bank management techniques to monitor the status of each SDRAM bank. Banks are only opened or closed when necessary, minimizing access delays.

For the controller, the data passes through the controller, and the controller handles all SDR related synchronization and timing generation. The controller separates the data in and data out bus at the FIFO interface.

The controller interface controller is provided with control registers for all timing parameters as well as memory configuration settings. This ensures compatibility with any SDRAM configuration.

The controller also provides low power management of SDRAM.

Feature List

The controller has the following features:

- SDR SDRAM and Mobile SDR SDRAM are supported.
- Compatible to JEDEC standard. The AMDDRC fully supports Micron, Samsung and Infineon devices, among others.
- Auto Low Power Management.
- Programmable CAS Latency: 1, 2 or 3 clock cycles.
- Memory data width is 16 bits
- Supports DQM operation.
- Supports Auto Refresh mode, Self Refresh mode and power-down mode.
- Supports all power-saving features (PASR, TCSR & Deep Power Down) for Mobile SDRAM.
- Programmable timing parameters. tWR, tWTR, tRCD, tRP, tMRD, tRFC, tXP, tXSR/tXSNR, tRFC

- NOP, READ, WRITE, AUTO REFRESH, ACTIVE, PRECHARGE, DPD, PD, SEFLREFRESH, LOAD MODE REGISTER commands are fully supported.
- Bank management logic monitors the status of each SDRAM bank. Bank only opened or closed when necessary, minimizing access delay.
- Automatically generates initialization sequence.

12 *SPI Interface*

ATJ2259B SPI can be configured as either a master or slave device. During an SPI transfer, data is shifted out and shifted in (transmitted and received) simultaneously. The SPI_SCK line synchronizes the shifting and sampling of the information. It is an output when the SPI is configured as a master or an input when the SPI is configured as a slave.

SPI uses a couple parameters called clock polarity (CPOL) and clock phase (CPHA) to determine when data is valid with respect to the clock signal. These must be set on the Master and all the Slaves in order for communication to work. CPOL determines whether the leading edge is defined to be the rising or falling edge of the clock (and vice versa for the trailing edge). CPHA determines whether the leading edge is used for setup or sample (and vice versa for the trailing edge). The following table summarizes the various settings:

SPI Settings

CPOL/CPHA	Leading Edge	Trailing Edge	SPI Mode
0/0	Sample, rising	Setup, falling	0
0/1	Setup, rising	Sample, falling	1
1/0	Sample, falling	Setup, rising	2
1/1	Setup, falling	Sample, rising	3

12.1 Registers List

SPI Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
SPI	0x10080000	0xB0080000

SPI Registers Offset Address

Offset	Register Name	Description
0x0000	SPI_CTL	SPI Control Register
0x0004	SPI_CLKDIV	SPI Clock Divide Register

0x0008	SPI_STAT	SPI Status Register
0x000c	SPI_RXDAT	SPI Receive FIFO Data Register
0x0010	SPI_TXDAT	SPI Transmit FIFO Data Register

12.2 Registers Description

12.2.1 SPI_CTL

SPI Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31:24	-	Reserved	R	0
23:22	RDIC	RX DRQ/IRQ Control. 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	0
21:20	TDIC	TX DRQ/IRQ Control. 00: set when TX FIFO is 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	0
19	TWME	Two wire mode enable bit 0: normal 4 wire mode 1: two wire mode, use two pin, SPI_CLK and SPI_MOSI	RW	0
18	EN	Enable. 0: Disable 1: Enable	RW	0
17:16	RWC	R/W control 00: no effect 01: write only 10: read only 11: write and read	RW	00

15	DTS	DMA transfer start（available only in master read only mode） 0: DMA transfer over.(this bit will be cleared to 0 when transfer over) 1: DMA transfer start(write 1 will start the DMA data transfer)	RW	0
14	SSATEN	SPI_SS active automatically enable when in mode 0 and mode 2 0:disable 1:enable	RW	0
13	RXBL	SPI RX DMA block mode enable 0: demand mode 1: block mode	RW	0
12	TXBL	SPI TX DMA block mode enable 0: demand mode 1: block mode	RW	0
11	-	Reserved	R	0
10	FMS	SPI fast mode select, only apply to SPI master mode. 0: synchronization design, SPICLK=HCLK/(CLKDIV*2), the least value of CLKDIV is 3, so the least divide is 6. 1: fast mode, SPICLK=HCLK/(CLKDIV*2), but when CLKDIV is set to 0, the divide is 1. so the least divide is 1.	RW	0
9	MS	Master/Slave Select. 0: Master 1: Slave	RW	0
8	DAWS	Data/Address Width. Select 0: 8 bit data and address 1: 16 bit data and address	RW	0
7:6	CPOS	Clock Polarity Select. CPOL CPHA 00: Mode 0 01: Mode 1 10: Mode 2 11: Mode 3	RW	b11
5	LMFS	LSB/MSB First Select. 0:Transmit and receive MSB first 1:Transmit and receive LSB first	RW	0
4	SSCO	SPI_SS Control Output(only for master mode). 1: output high	RW	1

		0: output low.		
3	TIEN	TX IRQ Enable. 0: Disable 1: Enable	RW	0
2	RIEN	RX IRQ Enable. 0: Disable 1: Enable	RW	0
1	TDEN	TX DRQ Enable. 0: Disable 1: Enable	RW	0
0	RDEN	RX DRQ Enable. 0: Disable 1: Enable	RW	0

Note:

1. The bit 14 is valuable only operation in the mode 0, mode2.
2. When the TMS=1 & RWC=10, the controller will automatically send the clock.
3. When the TMS=1 & RWC=11, the controller will send the clock depend on the data of register SPI_TXDATA.
4. When the data<4 bytes(8 bit mode), data<8 bytes(16 bit mode), the DMA mode should not used.
5. The select DMA mode or CPU mode depend on the [TDEN] and [RDEN].

12.2.2 SPI_CLKDIV

SPI Clock Divide Control Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9:0	CLKDIV	Depend on the SPI_CTL bit 10: SPICLK=HCLK/(CLKDIV*2), When not select fast mode, the least value of CLKDIV is 3, so the least divide from HCLK is 6. Supporting SPI clock rate up to 15MHz. When SPI master, select fast mode, the least value of CLKDIV is 0.when CLKDIV is set to 0, the divide is 1. so the least divide is 1. Supporting SPI clock rate up to 60MHz.	RW	0

12.2.3 SPI_STAT

SPI Status Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9	TFEM	TX FIFO Empty. 1: Empty 0: Not Empty	R	1
8	RFFU	RX FIFO Full. 1: Full 0: Not Full	R	0
7	TFFU	TX FIFO Full. 1: Full 0: Not Full	R	0
6	RFEM	RX FIFO Empty. 1: Empty 0: Not Empty	R	1
5	TFER	TX FIFO Error. When overflow, the bit is set to 1. Writing 1 to the bit will clear the bit and reset the FIFO.	RW	0
4	RFER	RX FIFO Error. When overflow, the bit is set to 1. Writing 1 to the bit will clear the bit and reset the FIFO.	RW	0
3	-	Reserved	R	0
2	TCOM	Transfer Complete Bit. DMA mode: bit will be set to 1 when all the data sent out CPU mode: will be set to 1 when very byte data sent out Write 1 will clear to zero	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit will clear it.	RW	0
0	PIP	RX IRQ Pending Bit. 0: No IRQ	RW	0

		1: IRQ Write 1 to this bit will clear it.		

Note

1. When the SPI_CTL [RWC] =11 and:

TX: DMA mode, RX: CPU mode

Or TX: CPU mode, RX: DMA mode

Than SPI_STA [TCOM] will be set to 1 when every byte data sent out.

12.2.4 SPI_RXDAT

SPI RXData Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	RXDAT	Receive Data. The depth of RXFIFO is 16bit×16 levels.	R	x

12.2.5 SPI_TXDAT

SPI TXData Register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:0	TXDAT	Transmit Data. The depth of RXFIFO is 16bit×16 levels.	W	x

13 *Nand Flash/SMC Interface*

The general purpose of Nand Flash Interface controller is a State Machine configurable interface to external Nand Flash/SMC. The highly configurable and flexible interface can attach to using most of readily available Nand Flash device.
The flash State machine provides automatic timing control for the using data read and write access signal line. The interface automatically maintains proper CLE, ALE and CE setup and hold up. The Controller will transfer the data between the Int_RAM Mem and ext_Flash Mem by AHB.

The Controller module can monitor the relatively interval transitions of the NAND flash device's Ready/Busy signal. This include an interrupt that can monitor the rising edge of the busy signal and that can be set generate a timeout interrupt if the NAND flash device hang up, etc.

The controller can support SLC/MLC NAND FLASH as well as Hamming ECC and 8bits and 12bits BCH ECC.

14 *SD/MMC/SDIO Controller*

This section is based on MMC card specification 4.2, and is compatible with SD memory card physical layer specification version 2.00. Multimedia Card/SD is serial input/output interface to send command and receive data. And it has 10 pin, such as, CMD, CLk, Data7~0, its feature as following

1. Support SD memory card, MMC memory card, INAND, MOVINAND, eMMC, CE-ATA Micro Drive, etc.
2. Support SDIO function
3. Support 1 bit, 4bit, 8bit, bus mode;
4. Clock max rate up to 52MHz.
5. Data transfer FIFO.
6. Read /Write CRC Status Hardware auto checked.
7. Support Auto Block mode.

15 *Memory Stick (MS)*

This document describes the Memory stick/pro/micro card controller. And it supports Memory stick stand format specification ver1.43, Memory stick PRO format specification ver1.02 and Memory Stick Micro Format specification ver1.01;

Electrical specification as following:

Signal pin:	6pin. Including Data0~3, CLK, BS.
Maximum transmission clock:	serial-20MHz; parallel-40MHz
Power source voltage:	2.7~3.6V
Maximum Capacity:	MS card-128MB; MS pro/micro-32GB

16 YUV2RGB/LDC

16.1 Block Description

This Module performs the image Data transfer from the frame buffer to LDC panel. It accelerates the frame data display by hardware operation. It is optional and mainly used in the movie decoding.

The process includes:

1. Up-sampling from YUV 422 to YUV 444
2. Change from YUV / YCbCr to RGB (8,8,8) format

YCbCr to RGB:

R = Y + 1.402 *(Cr-128)

G = Y - 0.34414*(Cb-128) - 0.71414*(Cr-128)

B = Y + 1.772 *(Cb-128)

YUV to RGB:

R = Y + 1.14V

G = Y - 0.39U - 0.58V

B = Y + 2.03U

3. Cut down RGB (8, 8, 8) to the RGB format which is needed in LDC Panel.

16.2 YUV2RGB Registers List

YUV2RGB Registers Block Base Address

Block Name	Physical Base Address	KSEG1 Base Adress
YUV2RGB	0x100F0000	0xB00F0000

YUV2RGB Registers Offset Address

Offset	Register Name	Description
0x0000	YUV2RGB_CTL	YUV2RGB Control Register
0x0004	YUV2RGB_FIFODAT	YUV2RGB FIFO Data Register
0x0008	YUV2RGB_CLKCTL	YUV2RGB Clock Control Register
0x000c	YUV2RGB_FrameCount	YUV2RGB Frame Count Register

16.3 YUV2RGB Registers Description

16.3.1 YUV2RGB_CTL

YUV2RGB Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0
20	WFBM	Write Fifo Block Mode 0: Normal Mode 1: Block Mode	RW	0
19	EN	RGB Decoder Enable. 0: Disable 1: Enable	RW	0
18	FES	Fifo Empty Status 0: Not Empty 1: Empty	R	1
17:16	WDCS	Write Data/Command Select 00:Write Command （Write LDC register address） 01:Write Data (Write LDC register data) 10:RGB(565) Data FrameBuffer Transfer 11:YCbCr/YUV Data FrameBuffer Transfer	RW	0
15	DEST	RGB Decoder Destination. 0: LDC interface 1: Frame buffer	RW	0
14	INS	Input YUV/YCbCr Select. 0: YCbCr 1: YUV	RW	0
13:11	FORMATS	RGB Format Select: 000: 16bit(RGB 565 1transfer) 001: 18bit(RGB 666 1transfer) 010: 8bit(RGB 565 2transfer) 011: 9bit(RGB 666 2transfer) 100: 8bit(RGB 888 3transfer) 101: 6bit(RGB 666 3transfer) 110: Reserved	RW	0

		111: Reserved		
10	SEQ	RGB Sequence. 0: RGB 1: BGR	RW	0
9	FWCS	FIFO Write Channel Select. 0: Special Channel 1: AHB Bus	RW	0
8	-	Reserved	R	0
7	EMDE	FIFO Empty (Write) DRQ Enable. 0: Disable 1: Enable	RW	0
6	EMIE	FIFO Empty (Write) IRQ Enable. 0: Disable 1: Enable	RW	0
5:4	-	Reserved	R	0
3	EMCO	FIFO Empty (Write) Condition. 0: 4/8 Empty 1: 0/8 Empty	RW	0
2	EMIP	FIFO Empty (Write) IRQ Pending Bit. 0: No IRQ 1: IRQ Write 1 to the bit, clear the bit.	RW	0
1:0	-	Reserved	R	0

Note: When RGB decoder destination (Bit15) selects LDC interface, LDC color depth can select RGB565 and RGB666 format.

When RGB decoder destination selects framebuffer, LDC color depth can only select RGB565 format.

16.3.2 YUV2RGB_DAT

YUV2RGB FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:0	DAT	FIFO Data.	RW	x

16.3.3 YUV2RGB_CLKCTL

YUV2RGB Clock Control Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:15	-	Reserved	R	0
14:8	RWCLKHDIV	R/W Clock High Cycle Division (from AHB Bus). Divide from 1~128	RW	0x7f
7	-	Reserved	R	0
6:0	RWCLKLDIV	R/W Clock Low Cycle Division (from AHB Bus) Divide from 1~128	RW	0x7f

16.3.4 YUV2RGB_FrameCount

YUV2RGB Frame Count Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:17	-	Reserved	R	0
16:8	FCOLC	Frame Column Counter.	RW	0
7:0	FROWC	Frame Row Counter.	RW	0

16.4 YUV2RGB Hardware Description

The YUV2RGB consists of the signals list which is as following:

Signal	Input/Output	Description
LDC_D[17:0]	O	18-bit parallel data output.
LDC_WRB	O	The same signal as WRB
LDC_RDB	O	The same signal as RDB
LDC_RS	O	Data / command select
LDC_CE	O	LCD-chip select

Interface DATA Format description:

WD0-WD17 and NAND/SD DATA Bus are multi-function pin.

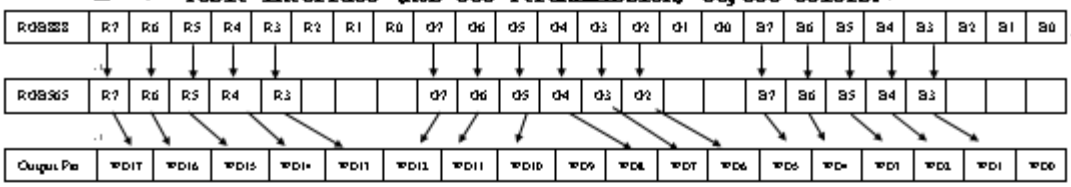
WD(0-17)	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0
D(0-15)	D15	D14	D13	D12	D11	D10	D9	D8		D7	D6	D5	D4	D3	D2	D1	D0	

a. If write command to LDC by 16bit mode, write display data can by both 16bit mode and 18bit mode in YUV2RGB decoder.

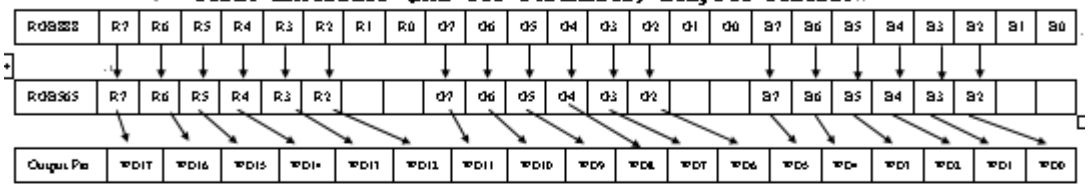
b. If write command to LDC by 8bit mode, write display data can 8bit mode and 6bit mode.

DATA Format Of RGB decoder interface

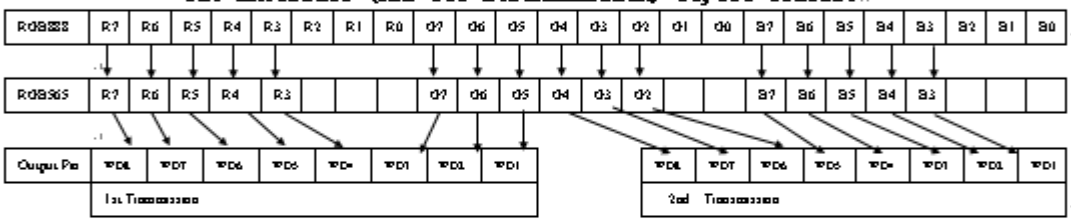
■ → 16bit interface (RGB 565 1transmission) 65,536 colors:



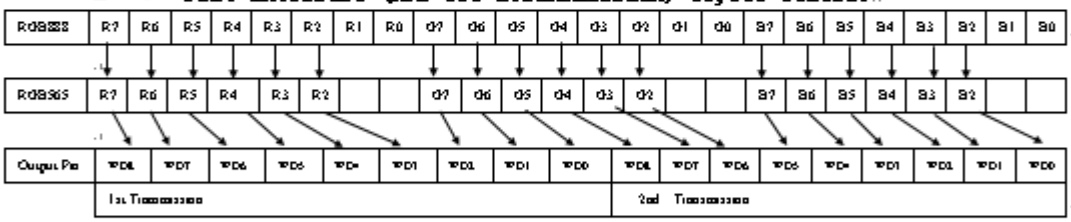
■ → 18bit interface (RGB 666 1transfer) 262,144 colors:



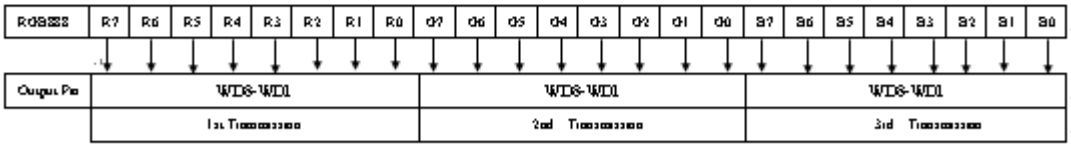
■ → 8bit interface (RGB 565 2transmission) 65,536 colors:



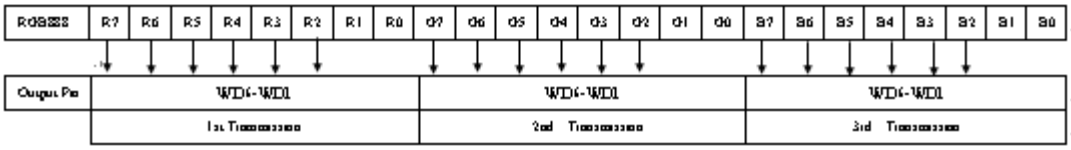
■ → 9bit interface (RGB 565 2transmission) 65,536 colors:



■ → 8bit interface (RGB 888 3transmission)



■ → 6bit interface (RGB 666 3transmission)



17 LDR Controller

17.1 Block description

17.1.1 Product Description

LDR timing controller described in this document is one part of ATJ2259B chip, which is a multimedia decoder IC. The controller is expected to drive digital RGB IF TFT LCD panels with pixel data output from DMA and programmed timing sequence.

LDR controller outputs synch signals, data clock, data enable and pixel data to LDR panel for image display.

17.1.2 Feature List

LDR controller has the following features:

- ✓ Support programmable synch signals timing, and adaptive to various LDR panels;
- ✓ Support multi format display data;

17.2 Registers List

LDR Controller Base Address

Name	Physical Base Address	KSEG1 Base Address
LDR_LCD	0x100F8000	0xB00F8000

LDR Controller Configuration Registers

Offset	Register Name	Description
0x0000	LCD_Ctrl0	LDR Control 0
0x0004	LCD_Size	LDR Screen Size
0x0008	LCD_Status	Status Register
0x000c	LCD_RGBTiming0	Panel interface timing register0
0x0010	LCD_RGBTiming1	Panel interface timing register1

0x0014	LCD_RGBTiming2	Panel interface timing register2
0x0018	LCD_Color	Panel default color
0x001c	LCD_PWM	Plus Width Modulation Setting
0x0028	LCD_FIFODAT	DMA destination address

17.3 Registers Description

17.3.1 LCD_Ctrl0

This register is mainly used to configure the controller to fit the specified RGB IF panel

LCD_Ctrl0

Offset=0x00

Bits	Name	Description	R/W	Default
31-20	-	Reserve	-	0
19	FWCS	FIFO Write Channel Select. 0: Special Channel 1: AHB Bus	R/W	0
18-16	I/F	Panel RGB Interface Type Select 000: Reserved 001: 18-bit parallel 010: 16-bit(5-6-5 format) parallel 011: 8-color mode parallel 100: 24-bit(8-8-8 format) serial 101: 18-bit(6-6-6 format) serial 110,111: Reserved Note: The unused pins of LD[23..0] should be in stable output state to avoid EMI. FOR RGB IF ONLY	R/W	0
15:13	CC_ODD	LDR color sequence configuration for odd line 000:RGB 001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other:Reserved	R/W	0

12:10	CC_EVEN	LDR color sequence configuration for even line 000: RGB 001:RBG 010:GRB 011:GBR 100:BRG 101:BGR Other:Reserved	R/W	0
09:08	PAD	Color padding to 32 bit/pixel 00: do not pad 01: pad X after 10: pad X before 11:Reserved For example: if CC_ODD=00 and PAD=01, then the serial output should be RGBX. FOR RGB IF ONLY	R/W	0
07:06	VOM	Video Output Mode 00: Drive the panel with all-0s pixel data 01: Drive the panel with all-1s pixel data 10: Drive the panel with video pixel data (fetch pixel data from FIFO) 11: Drive the panel with default color	R/W	0
05	Reserved	RESERVED	-	-
04:02	DF	DMA input data format 000: color 16-BPP (R:6/G:5/B:5) 001: color 16-BPP (R:5/G:6/B:5) 010: color 16-BPP (R:5/G:5/B:6) 011: color 16-BPP (Alpha:1/R:5/G:5/B:5) 100: color 16-BPP (R:5/G:5/B:5/Alpha:1) 101: color 24-BPP (Padding:8/R:8/G:8/B:8)/DE input 110: color 32-BPP (Alpha:8/R:8/G:8/B:8) 111:Reserved Note: alpha value is ignored by LDR controller	R/W	0
01	PS	Pixel sequence for 16BPP format	R/W	0
00	EN	Video Output Enable Enable the timing generator to drive the panel at the beginning of the frame. Note: During the display time (EN ==1), it's sampled only at the end of the vertical blanking period every	R/W	0

		frame. FOR RGB IF ONLY		

Notes:

PS=0

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P1															
P0															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

PS=1

Bit

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P0															
P1															
15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

Notes:

ps and df are double buffered registers. Their values are not valid until one frame end each time the values are revised.

17.3.2 LCD_Size

This register is mainly used to configure the size of the LDR.

LCD_Size Offset=0x04

Bits	Name	Description	R/W	Default
31:26	RESERVED	-	—	—
25:16	Y	Screen height (in pixels) for RGB IF/ frame size height for CPU IF Panel height is Y+1	R/W	0
15:10	RESERVED	-	—	—
09:00	X	Screen width (in pixels) for RGB IF/ frame size width for CPU IF Panel width is X+1	R/W	0

17.3.3 LCD_Status

This register reflects the status of the controller. It also contains the interrupt enable bits

LCD_Status Offset=0x08

Bits	Name	Description	R/W	Default
31	VBI	Vertical Blanking Interrupt Asserted during vertical no-display period every frame. Interrupt triggered at the beginning of blanking period	R/W	0
30	HBI	Horizontal Blanking Interrupt Asserted during horizontal no-display period every scan line. Interrupt triggered at the beginning of blanking period	R/W	0
29	AVSI	Active Video Display Interrupt Asserted during active video display time for each line, Interrupt triggered at the beginning of active period for each line	R/W	0
28	UDF	Input FIFO underflow Set when FIFO is empty	R/W	0
27	VBIE	Vertical Blanking Interrupt Enable 0: Disable 1: Enable	R/W	0
26	HBIE	Horizontal Blanking Interrupt Enable 0: Disable 1: Enable	R/W	0
25	AVSIE	Active Video Display Interrupt Enable 0: Disable 1: Enable	R/W	0
24	UDFIE	Input FIFO underflow Interrupt Enable 0: Disable 1: Enable	R/W	0
23:0	—	RESERVED	—	—

Note: The VBI is used for software to reconfigure and start a new DMA transfer when a frame is in its vertical blanking period. When software is interrupted by a VBI, it should reset the DMA, reconfigure and start it. Make sure that the vertical blanking period is long enough for the CPU to process the VBI interrupt routine.

17.3.4 LCD_RGBTiming0

This register determines dot clock and output signals' phase. It also can enable/disable the output of the panel driving signals

LCD_Timing0 Offset=0x0C

Bits	Name	Description	R/W	Default
31:8	-	RESERVED	-	-
7	Vsync_INV	Vsync Output Polarity Inversion	R/W	0
6	Hsync_INV	Hsync Output Polarity Inversion	R/W	0
5	DCLK_INV	DCLK Output Polarity Inversion	R/W	0
4	LDE_INV	LDE Output Polarity Inversion	R/W	0
3:0	-	RESERVED	-	-

Notes:

1. When we define the timing parameters, it often refers to Tpclk (short for "pixel cycle period"). In parallel output mode, Tpclk = Tldrdclk; in serial mode, Tpclk = Tldrdclk * 3.
2. When the setting of Polarity Inversion is '0', For Vsync_INV, it means that in Vertical Sync Pulse Period, the Vsync signal's level is '0'; For Hsync_INV, it means that in Horizontal Sync Pulse Period, the Hsync signal's level is '0'; For LDE_INV, it means that in Display Data Valid Period, the LDE signal's level is '1'; For DCLK_INV, it means that Display Data is active in DCLK's falling edge. When the setting of Polarity Inversion is '1', the situation is reversed.

17.3.5 LCD_RGBTiming1

This register specifies timing parameters of the horizontal sync signal

LCD_Timing1 Offset=0x10

Bits	Name	Description	R/W	Default
31:30	-	RESERVED	-	-
29:20	HSPW	Horizontal Sync Pulse Width (in pixels) Thspw = (HSPW+1) * Tpclk	R/W	0
19:10	HFP	Horizontal Front Porch (in pixels) Thfp = (HFP +1) * Tpclk	R/W	0
9:0	HBP	Horizontal Back Porch (in pixels) Thbp = (HBP +1) * Tpclk	R/W	0

17.3.6 LCD_RGBTiming2

This register specifies timing parameters of the vertical sync signal

LCD_Timing2 Offset=0x14

Bits	Name	Description	R/W	Default
31:29	Reserved	-	-	-
28:20	VSPW	Vertical Sync Pulse Width (in lines) Tvspw = (VSPW+1) * Thsync	R/W	0
19:10	VFP	Vertical Front Porch (in lines) Tvfp = (VFP +1) * Thsync	R/W	0
9:0	VBP	Vertical Back Porch (in lines) Tvbp = (VBP +1) * Thsync	R/W	0

17.3.7 LCD_Color

This register specifies panel's default color

LCD_Timing2 Offset=0x18

Bits	Name	Description	R/W	Default
31:24	Reserved	-	-	-
23:16	R	panel's default color R	R/W	0
15:8	G	panel's default color G	R/W	0
7:0	B	panel's default color B	R/W	0

17.3.8 LCD_PWM

This register configures the two PWM signal's cycle and duties, pwm clk have a range of 10-100K

LCD_PWM Offset=0x1C

Bits	Name	Description	R/W	Default
31:12	PWM_DIV	PWM Clock Divider Tpwm = 64*Tdclk * (PWM_DIV +1)	R/W	0
11:6	PWM1_DUTY	PWM1 Duty Ratio Th1 = (PWM1_DUTY +1)/ 64	R/W	0
5:0	PWM0_DUTY	PWM0 Duty Ratio	R/W	0

		Th0 = (PWM0_DUTY +1) / 64		

17.3.9 LCD_FIFODAT

LCD fifo address Offset=0x28

Bits	Name	Description	R/W	Default
31:00	FD	Fifo data	W	0

17.4 Pin Assignment

For RGB interface, the pixel data are output in different pins of the 24 bits pixel data. The pin mapping is illustrated by the table below:

Table: RGB mode data output pin assignment

Pin Name	Serial 8-bit Bus						Parallel 24-bit Bus		
	18-bit			24-bit			8-color	16-bit	18-bit
	1st	2nd	3rd	1st	2nd	3rd			
LD[0]				R0	G0	B0			
LD[1]				R1	G1	B1			
LD[2]	R0	G0	B0	R2	G2	B2			B0
LD[3]	R1	G1	B1	R3	G3	B3		B0	B1
LD[4]	R2	G2	B2	R4	G4	B4		B1	B2
LD[5]	R3	G3	B3	R5	G5	B5		B2	B3
LD[6]	R4	G4	B4	R6	G6	B6		B3	B4
LD[7]	R5	G5	B5	R7	G7	B7	Bmsb	B4	B5
LD[10]								G0	G0
LD[11]								G1	G1
LD[12]								G2	G2
LD[13]								G3	G3
LD[14]								G4	G4
LD[15]							Gmsb	G5	G5
LD[18]									R0
LD[19]								R0	R1
LD[20]								R1	R2
LD[21]								R2	R3
LD[22]								R3	R4
LD[23]							Rmsb	R4	R5

18 *DAC, I2S Port and Headphone Driver*

ATJ2259B's internal DAC is an on-chip Sigma-Delta Modulator, a 18 bit high performance DAC is composed of it. The DAC interface support 8-level play back FIFO (16 X 24bits PCM data for L/R channel and variable sample rates, such as 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz.In I2S output mode,the FS can be surported up to 96k. An on-chip PLL2 is used to generate 22.5792MHz from 24MHz to support 44.1K/22.05K/11.025KHz with 256×FS clock for over-sampling, while 24MHz supports 48K/32K/24K/16K/12K/8KHz with 256×FS for over-sampling.

In I2S input mode, the master clock supports 256*FS or 384*FS.The sample data bit length is less than 24bit.The FS support up to 96k.

19 *ADC*

The internal microphone amplifier has gain for recording. The VMIC pin is the power supply (2.57V) for microphone, and the high voltage source for touch panel. The VLAD pin is the low voltage source for touch panel. They all need an external CAP for stability.

The audio ADC is a 21 bits sigma delta Analog-to-Digital Converter. Its input source can be selected from MIC amplifier or external FM or line-in, and it has two FIFO.

The Fs supports 48K/44.1K/32K/24K/22.05K/16K/12K/11.025K/8KHz.

20 SPDIF Interface

20.1 SPDIF Registers List

SPDIF Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
SPDIF	0x10140000	0xB0140000

SPDIF Registers Offset Address

Offset	Register Name	Description
0x0000	SPDIF_CTL	SPDIF Control Register
0x0004	SPDIF_STAT	SPDIF Status Register
0x0008	SPDIF_TXDAT	SPDIF TX FIFO Data Register
0x000c	SPDIF_RXDAT	SPDIF RX FIFO Data Register
0x0010	SPDIF_TXCSTAT	SPDIF TX Channel Status Register
0x0014	SPDIF_RXCSTAT	SPDIF RX Channel Status Register

20.2 SPDIF Registers Description

20.2.1 SPDIF_CTL

SPDIF Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15	EN	SPDIF Enable. 0: Disable (will reset the RX and TX state machine) 1: Enable	RW	0
14	TRFS	SPDIF TX/RX FIFO Select. 0: RX FIFO 1: TX FIFO	RW	0

13:12	-	Reserved	R	0
11:10	TDIC	SPDIF TX DRQ/IRQ Control. X0:set when FIFO is empty X1:set when FIFO is half empty In DMA DRQ mode,this field must be set X1. In DMA mode,TX fifo empty is at least 2 bytes remained.	RW	0
9:8	RDIC	SPDIF RX DRQ/IRQ Control. X0:set when FIFO is half full X1:set when at least one byte is received In DMA DRQ mode,this field must be set X0.	RW	0
7	TXDE	SPDIF TX DRQ Enable. 0: Disable 1: Enable	RW	0
6	RXDE	SPDIF RX DRQ Enable. 0: Disable 1: Enable.	RW	0
5	TXIE	SPDIF TX IRQ Enable. 0: Disable 1: Enable.	RW	0
4	RXIE	SPDIF RX IRQ Enable. 0: Disable 1: Enable.	RW	0
3	BIE	SPDIF Block IRQ Enable. 0: Disable 1: Enable	RW	0
2	TXFR	SPDIF TX FIFO Reset. (also reset the TX state machine). 0: FIFO reset valid 1: FIFO reset invalid.	RW	0
1	RXFR	SPDIF RX FIFO Reset. (also reset the RX state machine). 0: FIFO reset valid 1: FIFO reset invalid	RW	0
0	-	Reserved	RW	0

20.2.2 SPDIF_STAT

SPDIF Status Register
Offset=0x0004

Bits	Name	Description	R/W	Reset
31:18	-	Reserved	R	0
17	TFES	TX FIFO empty Status 0: empty 1: no empty	R	0
16	RFFS	RX FIFO full Status 0: no full 1: full	R	0
15:12	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0
11:10	-	Reserved	R	0
9:8	SAMRD	Sample Rate Detected. 00:44.1 kHz 01:DC 10:48 kHz 11:32 kHz	R	0
7	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
6	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
5	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
4	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0
3	BIP	SPDIF Block IRQ Pending Bit. (receive the B preamble) 0: No IRQ 1: IRQ Writing 1 to this bit will clear it.	RW	0
2	TFEP	TX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to this bit will clear it or reset FIFO clear it.	RW	0

1	RFEP	RX FIFO Error Pending Bit. 0: No Error 1: Error Writing 1 to this bit will clear it or reset FIFO clear it.	RW	0
0	RERP	Receive Error Pending Bit. 0: No Error 1: Error Writing 1 to this bit will clear it.	RW	0

20.2.3 SPDIF_ TXDAT

SPDIF TX FIFO DATA Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:26	-	Reserved	R	0
25:0	TXDAT	SPDIF TX FIFO DATA. Note: bit[23:0] is the really send data.	W	x

20.2.4 SPDIF_ RXDAT

SPDIF RX FIFO DATA Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:26	-	Reserved	R	0
25:0	RXDAT	SPDIF RX FIFO DATA. The depth of TX FIFO is 26bit x 8 levels. Note: bit [23:0] is the really received data. Bit[25:24] is the data type 00:B 01:W 10:M 11:Reserved	R	x

20.2.5 SPDIF_ TXCSTAT

SPDIF TX Channel Status Register

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:0	TXCSTAT	SPDIF TX Channel Status.	RW	x

Notes:

For TX:

There is not channel status CRC to transfer. Here the SPDIF_TXSTAT just mapped to first 32 bit of every 192 frames data and the remained bit will be set to zero by the hardware.

20.2.6 SPDIF_ RXCSTAT

SPDIF RX Channel Status Register

Offset=0x14

Bits	Name	Description	R/W	Reset
31:0	RXCSTAT	SPDIF RX Channel Status.	RW	x

Notes:

For RX:

There are 192 bits status data per 192 frames transfer. The SPDIF_RXSTAT register only receive the bit 32 bit data ever 192 frames data of the left channel status.

20.3 SPDIF Signals Description

The SPDIF Interface consists of the signals list which is as following:

Signal	Input/Output	Description
SPDIF_TX	O	SPDIF Transmit.
SPDIF_RX	I	SPDIF Receive.

21 *UART (2) Interface*

21.1 Block Description

ATJ2259B Platform contains two UART interfaces. Each UART has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Interrupts for Receive FIFO Half Full and Not Empty
- Interrupts for Transmit FIFO Empty and Half Empty
- Support RTS/CTS Automatic Hardware Flow Control on UART1 to reduce interrupts to host system
- Capable of speeds up to 1.5Mbs to enable connections with Bluetooth and other peripherals
- UART2 has Infrared Data Association(IrDA) Inputs and Outputs (Optional)

UART1BaudRate

The UART Baud Rate must be selected by setting the UART1_CLK_Con Register of the CMU.

UART1BauRate*8=S_CLK/UART1_CLK_DIV

21.2 UART Registers List

Each UART is controlled by a register block.

Uart Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
Uart1	0x10160000	0xB0160000
Uart2	0x10160020	0xB0160020

Each register block contains the registers.

UART Registers Offset Address

Offset	Register Name	Description
0x0000	UARTx_CTL	UART Control Register

0x0004	UARTx_RXDAT	UART Receive FIFO Data Register
0x0008	UARTx_TXDAT	UART Transmit FIFO Data Register
0x000c	UARTx_STAT	UART Status Register

21.3 UART Registers Description

21.3.1 UART1_CTL

UART1 Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:20	-	Reserved	RW	0
19	TXIE	UART1 TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART1 RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART1 TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART1 RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART1 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0
14	TRFS	UART1 TX/RX FIFO Select TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART1_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set.	RW	0

12	AFE	Autoflow Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals.	RW	0
11:10	RDIC	UART1 RX DRQ/IRQ Control 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
9:8	TDIC	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is 1 byte leave in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
7	BLOC	Uart1 DMA block mode Enable 0:demand 1:Block	RW	0
6:4	PRS	Parity Select. Bit 4: EPS, Even parity Bit 5: STKP, Stick parity Bit 6: PEN, Parity enable PEN EPS STKP Selected Parity 0 x x None 1 0 0 Odd 1 0 1 Even 1 1 0 logic 1 1 1 1 logic 0	RW	000
3	-	Reserved	R	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	RW	0
1:0	DWLS	Data Width Length Select.	RW	00

		00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits		

Notes

1. The Uart module should be reset when the next time usage.

21.3.2 UART1_RXDAT

UART1 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8:0	RXDAT	Received Data. The depth of FIFO is 9bit×8 levels. The 8th bit is the error bit	R	x

21.3.3 UART1_TXDAT

UART1 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	TXDAT	Received Data. The depth of FIFO is 8bit×16 levels	R	x

21.3.4 UART1_STAT

UART1 Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:16	-	Reserved	R	0
15:11	TRFL	TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0

10	TFES	TX FIFO empty Status 0: empty 1: no empty	R	0
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	RTSS	RTS Status. The bit reflects the status of the external RTS- pin.	R	x
7	CTSS	CTS Status. The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP	TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0
0	RIP	RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

Notes

1. Software should reset the Uart module when some error information is detected.

21.3.5 UART2_CTL

UART2 Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31:24	-	Reserved	R	0
23	PWS	SIR pulse width select 0: 3/16 bit width 1: 1.6us width, (support baudrate from 9600 to 115200 bps)	RW	0
22	IRTR	IR TX Reverse bit , 0 disable; 1 enable	RW	0
21	IRRR	IR RX Reverse bit , 0 disable; 1 enable	RW	0
20	-	Reserved	RW	0
19	TXIE	UART2/IR TX IRQ Enable. 0: Disable 1: Enable	RW	0
18	RXIE	UART2/IR RX IRQ Enable. 0: Disable 1: Enable	RW	0
17	TXDE	UART2/IR TX DRQ Enable. 0: Disable 1: Enable	RW	0
16	RXDE	UART2/IR RX DRQ Enable. 0: Disable 1: Enable	RW	0
15	EN	UART2/IR Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state.	RW	0
14	TRFS	TX/RX FIFO Select. TX/RX FIFO Level is reflected in bit 15 to bit 12 of UART2_STAT Register. 0: RX FIFO 1: TX FIFO	RW	0
13:12	MS	Mode Select. 00: UART2 01: IRDA-SIR 10: IRDA-MIR	RW	0

		11: IRDA-FIR		
11:10	RDIC	UART2 RX DRQ/IRQ Control 00: set when at least one byte received in IRQ mode. 01: set when 4 bytes received in IRQ/DRQ mode 10: set when 8 bytes received in IRQ/DRQ mode 11: set when 12 bytes received in IRQ/DRQ mode In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
9:8	TDIC	UART2 TX DRQ/IRQ Control 00: set when TX FIFO is 1 byte leave in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ/DRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, because at lease 2 bytes necessary.	RW	00
7	BLOC	Uart2 DMA block mode Enable 0:demand 1:Block	RW	0
6:4	PRS	Parity Select. Bit 4: EPS, Even parity Bit 5: STKP, Stick parity Bit 6: PEN, Parity enable PEN EPS STKP Selected Parity 0 x x None 1 0 0 Odd 1 0 1 Even 1 1 0 logic 1 1 1 1 logic 0	RW	0
3	VFIRE	VFIR Function enable 0: disable 1: enable	RW	0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. The receiver always checks 1 stop bit only.	RW	0
1:0	DWLS	Data Width Length Select.	RW	00

		00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits		

Notes

1. The Uart module should be reset when the next time usage.

21.3.6 UART2_RXDAT

UART2 Receive FIFO DATA Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:10	-	Reserved	R	0
9:0	RXDAT	UART2/IR Received Data. The depth of FIFO is 10bit×16 levels. The 9th bit is the error bit, the 8th bit is the end of package bit and the 7:0 bits is the data.	R	x

21.3.7 UART2_TXDAT

UART2 Transmit FIFO DATA Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8:0	TXDAT	UART2/IR Transmit Data. The depth of FIFO is 9bit×16 levels. The 8th bit is the end of package bit and the 7:0 bits is the data.	W	x

21.3.8 UART2_STAT

UART2 Status Register

Offset=0x000c

Bits	Name	Description	R/W	Reset

31:16	-	Reserved	R	0
15:11	TRFL	UART2/IR TX/RX FIFO Level. The field indicates the current RX and TX FIFO level.	R	0
10	TFES	TX FIFO empty Status 0: empty 1: no empty	R	0
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0
8	IRES	IR EOP Status. Writing the bit to high when next writing IR TX FIFO is the last byte of the packet. Next writing TX FIFO after this bit is set will clear this bit automatically. When read from this bit, the EOP status bit of IR receiver is returned. This bit can be polled by MCU to see if end of package is reached.	RW	0
7	IRCE	IR CRC Error Flag Bit(only in MIR or FIR mode). write 1 to this bit will clear it.	RW	0
6	TFFU	UART2/IR TX FIFO Full. 1: Full 0: No Full	R	0
5	RFEM	UART2/IR RX FIFO Empty. 1: Empty 0: No Empty	R	1
4	RXST	UART2/IR Receive Status. 0: receive OK 1: receive error. Writing 1 to the bit will clear the bit.	RW	0
3	TFER	UART2/IR TX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the TX FIFO.	RW	0
2	RXER	UART2/IR RX FIFO Error. 0: No Error 1: Error Writing 1 to the bit will clear the bit and reset the RX FIFO.	RW	0
1	TIP	UART2/IR TX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear the bit.	RW	0

0	RIP	UART2/IR RX IRQ Pending Bit. 0: No IRQ 1: IRQ Writing 1 to the bit to clear it.	RW	0

Notes

1. Software should reset the Uart module when some error information is detected.

21.4 UART Signals Description

The UART Interface consists of the signals list which is as following:

Signal	Input/Output	Description
UART1		
UART1_TX	O	UART1 Transmit.
UART1_RX	I	UART1 Receive.
UART1_CTSB	I	Clear to Send.
UART1_RTSB	I	Ready for Data Set.
UART2		
UART2_TX	O	UART2 Transmit.
UART2_RX	I	UART2 Receive.

22 IR Interface

22.1 Block Description

IrDA is a standard defined by the IrDA consortium (Infrared Data Association). It specifies a way to wirelessly transfer data via infrared radiation. The IrDA specifications include standards for both the physical devices and the protocols the use to communicate with each other. IrDA devices conforming to standards IrDA 1.0 and 1.1 works over distances.

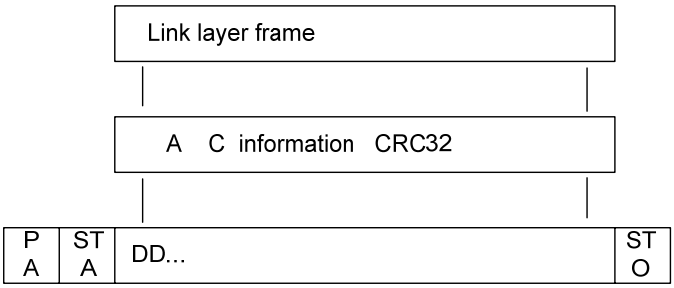
Speeds for IrDA v1.0 range from 2400 to 115200 bps. Pulse modulation with 3/16 of the length of the original duration of a bit is used. Data format is the same as for a serial port asynchronously transmitted word, with a start bit at the beginning.

IrDA v1.1 defines speeds 0.576 and 1.152 Mbps for MIR mode and 4Mbps for FIR mode, with 1/4 mark-to-space ratio.

For MIR mode, the basic unit (packet) is transmitted synchronously, with a starting sequence at the beginning. A packet consists of two start words followed by target address (IrDA devices are assigned numbers by the means of IrDA protocol, so they are able to unambiguously identify themselves), data, CRC-16 and a stop word.

STA: Beginning Flag, 01111110 binary
ADDR: 8 bit Address Field
DATA: 8 bit Control Field plus up to 2045=(2048-3) bytes information Field
FCS: CCITT 16 bit CRC
STO: Ending Flag, 01111110 binary

For FIR mode, two bits are encoded in a pulse within one of the four possible positions in time. So, information is carried by the pulse position, instead of pulse existence as in previous modulations. With bit speed of 4Mbps, the transmitter flashed at 2MHZ rate. However, unlike 0.576 and 1.152 Mbps, 4Mbps packets use CRC-32 correction code.



Support SIR, MIR and FIR mode.

16-bit and 32-bit hardware CRC generation and detection.

You can't use the UART2 and IR at the same time because IR an UART2 have some common register.

The UART/IR baud Rate must be selected by setting the UART2_CLK_Con Register of the CMU.

Table: IrDA mode supported

Mode	Speed	CLK setting	Compliance
SIR	2.4 to 115.2kbps	Depend on the UART2_CTL bit 23: When select pulse width 3/16 bit : BaudRate*16=CORE_CLK/UART2_CLK_DIV When select pulse width 1.6u, (support baudrate from 9600 to 115200 bps) BaudRate*16*16= CORE_CLK/UART2_CLK_DIV	IrDA 1.0
MIR	0.576 and 1.152 Mbps	BaudRate*8=CORE_CLK/UART2_CLK_DIV	IrDA 1.1 with error detection
FIR	4 Mbps	24M=CORE_CLK/UART2_CLK_DIV	IrDA 1.1 with error detection

22.2 IR Registers List

IR Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
IR	0x10160000	0xB0160000

IR Registers Offset Address

Offset	Register Name	Description
0x0030	IR_PL	IrDA Packet Length Register
0x0034	IR_RBC	IrDA Receive Byte Count Register

22.3 IR Registers Description

22.3.1 IR_PL

IrDA Packet Length Register
Offset=0x0010

Bits	Name	Description	R/W	Reset
31:13	-	Reserved	R	0
12:0	MAXSPL	Maximum Send Packet Length (Only used in MIR or FIR mode).	RW	0

22.3.2 IR_RBC

IrDA Receive Byte Count Register
Offset=0x0014

Bits	Name	Description	R/W	Reset
31:13	-	Reserved	R	0
12:0	CRXBN	Current Received Bytes Number (Only used in MIR or FIR mode). Writing the field to reset it.	RW	0

23 I2C (2) Interface

23.1 Block Description

ATJ2259B has two I2C Interface, which can be configured as either master or slave device. In master mode, it generates the clock (I2C_SCL) and initiates transactions on the data line (I2C_SDA). Data on the I2C bus is byte oriented. Multi-Master mode, 10-bit address and Hi-speed mode are not supported. See the I2C_Bus_Specification_1995 for detailed information.

Pull-up resistors are required on both of the I2C lines as all of the I2C drivers are open drain. Typically external 2k-Ohm resisters are used to pull the signals up to VCC.

23.2 I2C Registers List

Each I2C is controlled by a register block.

I2C Register Block Base Address

Block Name	Physical Base Address	KSEG1 Base Adress
I2C1	0x10180000	0xB0180000
I2C2	0x10180020	0xB0180020

Each register block contains the registers.

I2C Registers Offset Address

Offset	Register Name	Description
0x0000	I2Cx_CTL	I2Cx Control Register
0x0004	I2Cx_CLKDIV	I2Cx Clock Divide Register
0x0008	I2Cx_STAT	I2Cx Status Register
0x000c	I2Cx_ADDR	I2Cx Address Register
0x0010	I2Cx_DAT	I2Cx Data Register

23.3 I2C Registers Decription

23.3.1 I2Cx_CTL

I2Cx Control Register
Offset=0x0000

Bits	Name	Description	R/W	Reset
31:9	-	Reserved	R	0
8	PUEN	Internal Pull-Up Resistor(4.7k) Enable. 0: Disable 1: Enable	RW	0
7	EN	Enable. 0: Disable 1: Enable	RW	0
6	SIE	START Condition Generates IRQ Enable(only for slave mode). 0: Disable 1: Enable	RW	0
5	IRQE	IRQ Enable. 0: Disable 1: Enable	RW	0
4	MS	Mode Select. 0: Master mode 1: Slave mode	RW	0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition	RW	0
1	RB	Release Bus. Writing 1 to this bit will release the clock and data line to idle. MCU should write 1 to this bit after transmitting or receiving the last bit of a whole transfer.	RW	0
0	GRAS	Generating/Receiving Acknowledge Signal. In receive mode: 0: Generating the ACK signal to the transmitter at 9th clock of SCL 1: Don't generate the ACK signal at 9th clock of SCL	RW	0

		In transmit mode: 0: Has not received the ACK signal 1: Has received the ACK signal. This bit will be cleared when the 9th clock of next SCL arrived		

23.3.2 I2Cx_CLKDIV

I2Cx Clock Divide Control Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	CLKDIV	Clock Divider Factor (only for master mode). I2Cx clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=PCLK/(CLKDIV*16)	RW	0

23.3.3 I2Cx_STAT

I2Cx Status Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7	TRC	Transmit/Receive Complete Bit. The bit is automatically set when the buffer is empty in transmit mode or when the buffer is full in receive mode. Writing 1 to this bit will clear it. In transmit mode: 0: Transmit in progress 1: Transmit complete In receive mode: 0: Receive in progress 1: Receive complete	RW	0

6	STPD	STOP Detect Bit. The bit will be cleared when the I2C mode is disable or when the START condition is detected again. Writing 1 to the bit will clear it. 1: Indicate that the STOP bit is detected 0: STOP bit is not detected	RW	0
5	STAD	START Detect Bit. The bit is cleared when the I2C mode is disable or when the STOP condition is detected. Writing 1 to the bit will clear it. 1: Indicate that the START bit is detected 0: START bit is not detected	RW	0
4	RWST	Read/Write Status Bit(only for Slave mode). When in slave mode, this bit reflects the master device read from or write to the slave device if the last address is matched. This bit is valid before the next start bit, stop bit or NAK bit occurred. 1: Read 0: Write	RW	0
3	LBST	Last Byte Status Bit. 1: Indicate the last byte received or transmitted is data 0: Indicate the last byte received or transmitted is address	RW	0
2	IRQP	IRQ Pending Bit. Writing 1 to this bit will clear it. 1: IRQ 0: No IRQ	RW	0
1	OVST	Overflow Status Bit. Writing 1 to this bit will clear it. 1: A new byte is receiving while the previous byte has not been read 0: No overflow	RW	0
0	WCO	Writing Collision Bit. Writing 1 to this bit will clear it. 1: The I2C data register is written while it is still transmitting the previous byte 0: No collision	RW	0

Note: Whenever writing collision or overflow is set, NAK will occur automatically.

23.3.4 I2Cx_ADDR

I2Cx Address Register
Offset=0x000C

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:1	SDAD	Slave Device Address. In master mode,these bit are I2C slave device address. In slave mode,these bit is used to compare with the address that the master device sents out.	RW	0
0	RWCM	Read/Write Control or Match. In master mode, the bit is read/write control bit. 0: Write 1: Read In slave mode, the bit is slave address match bit. 0: Not match, don't send the IRQ 1: Match and will send IRQ to MCU	RW	0

23.3.5 I2Cx_DAT

I2Cx Data Register
Offset=0x0010

Bits	Name	Description	R/W	Reset
31:8	-	Reserved	R	0
7:0	TXRXDAT	Transmit/Receive Data.	RW	0

23.4 I2C Signals Description

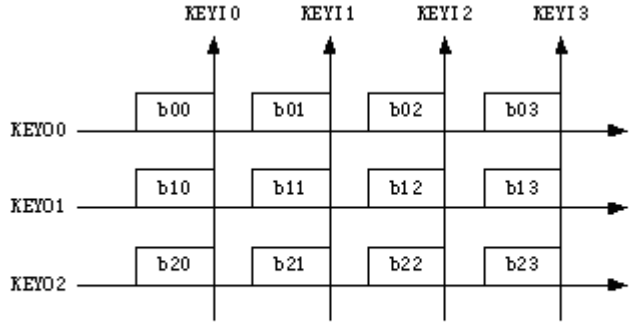
The I2C Interface consists of the signals list which is as following:

Signal	Input/Output	Description
I2Cx_SCL	I/O	I2C Clock Input/Output. When in master mode, the pin is output. When in slave mode, the pin is input.
I2Cx_SDA	I/O	I2C Data Input/Output.

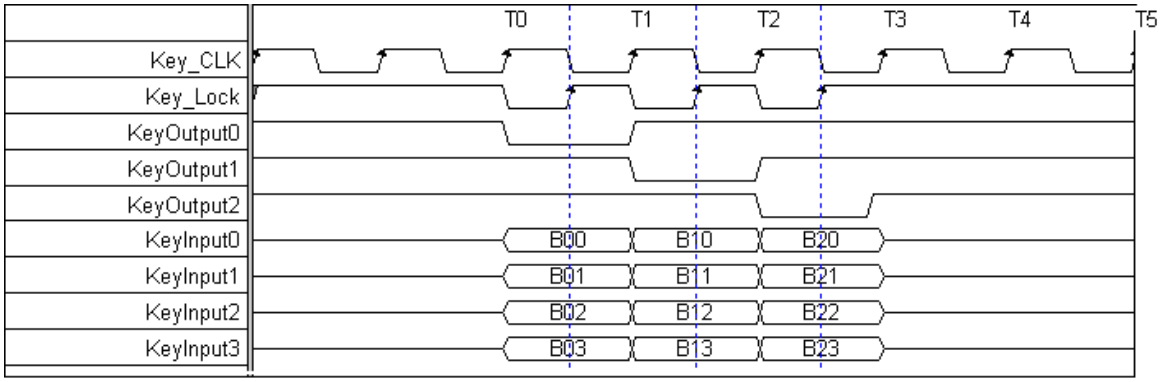
24 *Key Scan*

24.1 Block Description

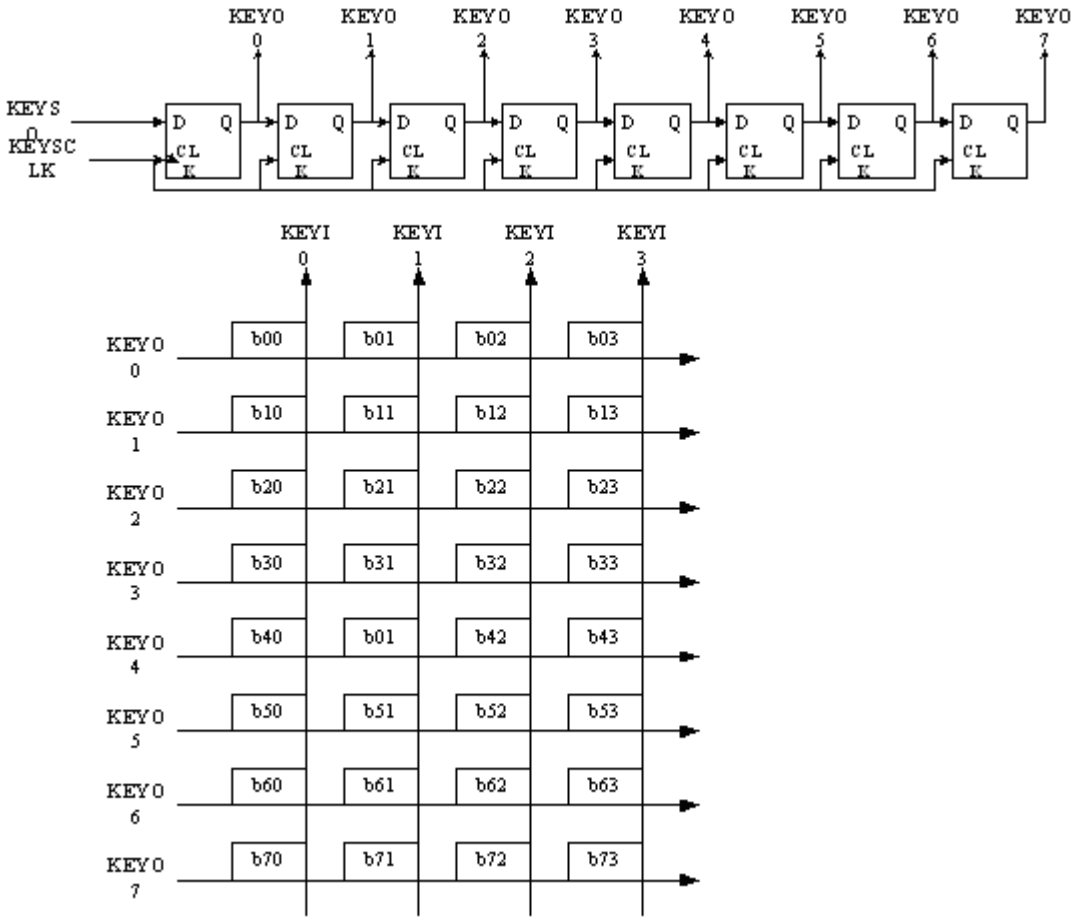
The Key Scan support parallel mode and searial mode. In parallel mode, ATJ2259B surport max scan matrixis 3*4, as follow:



Timing:

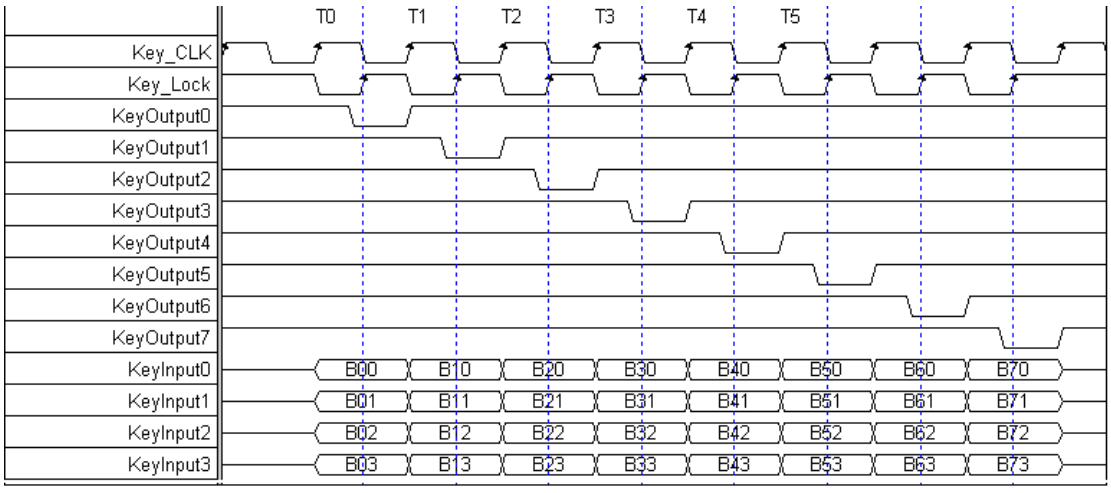


In serial mode, one or more external shift register chips should be used. The following is a 4*8 scan matrix.



Note: KEYSO is PIN KEYO1, KEYSCLK is PIN KEYO0.

The whole timing is below.



In serial mode, at last two external 8-bit shift registers can be used.That is to say, the maxium scan matrix is 4*16.

24.2 Key Scan Registers List

Key Scan Registers Block Base Address

Block Name	Physical Bass Address	KSEG1 Base Adress
KEY	0x101A0000	0xB01A0000

Key Scan Registers Offset Address

Offset	Register Name	Description
0x0000	KEY_CTL	Key Scan Control Register
0x0004	KEY_DAT0	Key Scan Data Register0
0x0008	KEY_DAT1	Key Scan Data Register1
0x000c	KEY_DAT2	Key Scan Data Register2
0x0010	KEY_DAT3	Key Scan Data Register3

24.3 Key Scan Registers Description

24.3.1 KEY_CTL

Key Scan Control Register

Offset=0x0000

Bits	Name	Description	R/W	Reset
31:27	-	Reserved	R	0
26:24	WTS	Key Scan Wait Time Select. KeyScan Wait Time=WTS*32ms	RW	0
23:20	KOUTEN	Key Scan output (KEYO[3:0])enable bit 0:Mask Key scan output 1: Enable Key scan output These bits are available for Parallel/Serial Mode	RW	0
19	OTYP	KSOUT pin output type,Only for Parrel Key mode 0:Open drain output. 1:push pull output	RW	0
18	IRCL	Key Scan IRQ Cleared (only used when shutting down APB Clock).	R	0
17	IRP	Key Scan IRQ Pending Bit. 0: No IRQ	RW	0

		1: IRQ Writing 1 to the bit will clear the bit.		
16	IREN	Key Scan IRQ Enable. 0: Disable 1: Enable	RW	0
15:8	INMKEN	Key Scan Input (KEYI [7:0]) Mask Enable. 0: Mask Key Input 1: Enable Key Input When any pin of KEYI [7:0] is masked, it can used as GPIO, even if key scan mode is active.	RW	0
7:6	MATS	Key Scan Matrix Select (Only active in serial mode). 00: 8*4. Use Key_DAT0 register. 01: 8*8. Use Key_DAT0 and Key_DAT1 registers. 10: 8*16. Use registers from Key_DAT0 to Key_DAT3 11: Reserved	RW	0
5:4	PRS	Key Scan Period Select. 00: 40ms 01: 80ms 10: 160ms 11: 320ms	RW	0
3:2	DTS	Key Scan Debounce Time Select. 00: 10ms 01: 20ms 10: 40ms 11: No debounce time The decounce time is 24MHz dividing frequency.	RW	0
1	MS	Key Scan Mode Select. 0: Parrel Mode 1: Serial Mode	RW	0
0	EN	Key Scan Enable. 0: Disable 1: Enable	RW	0

24.3.2 KEY_DAT0

Key Scan Data Register0
Offset=0x0004

Bits	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data.	R	x

24.3.3 KEY_DAT1

Key Scan Data Register1

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data.	R	x

24.3.4 KEY_DAT2

Key Scan Data Register2

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data.	R	x

24.3.5 KEY_DAT3

Key Scan Data Register3

Offset=0x0010

Bits	Name	Description	R/W	Reset
31:0	DAT	Key Scan Data.	R	x

25 GPIO_MFP

25.1 Block Description

There are 64 bit General purpose IO port in ATJ2259B. Each GPIO is controlled by corresponding bit in GPIOx_Out_En reg and GPIOx_In_En reg.
There many multi function pin in ATJ2259B. The register Multi_con0, Multi_con1 and Multi_con2 can control the pad's function. Some special pad with build-in pulls up or pulls down resistance.

25.1.1 Uart/IR/I2C/SPI/SPDIF

The UART, IR, I2C, SPI, SPDIF port share the pads. At one time only one controller can drive the pad. Software must assure this point.

25.1.2 GPIO/Function Pin

There are 64 gpios in ATJ2259B. GPIO share pads with many functional Pads. The GPIO function has the highest priority. That is to say, if gpio enabe input or output, the corresponding functional signal is masked.

25.1.3 RGB/Function Pin

CPU/parallel RGB/Serial RGB interfaces of LCD are supported. CPU interface of LCD shares NAND/SD data bus, while parallel RGB/Serial RGB interface of LCD shares Function pins. RGB interface has higher priority than function, but its priority is lower than GPIO. RGB interface includes data, control signals and 2 PWM signals.

25.1.4 Pad with Build-in Resistance

1, SD data bus:
SD_D0~D7, SD_CMD, pull up 50k
2, NF
NF_RB 2.2k pull up

3, I2C

SDA, SCL 4.7k pull up

4, keyin

600k pull up

5, MS data bus, MS clk, MS_bs

50k pulls down

6, SIRQ

SIRQ0 and SIRQ1 have 100k pull-up or 100k pull-down resistance. The type of resistance is controlled by config in external interrupt register. When "High level active" or "rising edge-triggered" is selected, pull-down resistance is active. While "Low level active" or "falling edge-triggered" is selected, pull-up resistance is active.

25.2 GPIO Registers List

GPIO Registers Block Base Address

Module name	Physical Bass Address	KSEG1 Base Adress
GPIO	0x101C0000	0xB01C0000

GPIO Registers Offset Address

Offset	Register Name	Description
0x0000	GPIO_AOUTEN	GPIOA Output Enable Register
0x0004	GPIO_AINEN	GPIOA Input Enable Register
0x0008	GPIO_ADAT	GPIOA Data Register
0x000c	GPIO_BOUTEN	GPIOB Output Enable Register
0x0010	GPIO_BINEN	GPIOB Input Enable Register
0x0014	GPIO_BDAT	GPIOB Data Register
0x0020	GPIO_MFCTL2	Multi Function Control Register2
0x0088	PAD_DRV	PAD Driver control Register

25.3 GPIO Registers Description

25.3.1 GPIO_AOUTEN

GPIOA Output Enable Register

Offset=0x0000

Bits	Name	Description	R/W	Reset

31:0	OUTEN	GPIOA[31:0] Output Enable. 0: Disable 1: Enable	RW	0

25.3.2 GPIO_AINEN

GPIOA Input Enable Register

Offset=0x0004

Bits	Name	Description	R/W	Reset
31:0	INEN	GPIOA [31:0] Input Enable. 0: Disable 1: Enable	RW	0

25.3.3 GPIO_ADAT

GPIOA Data Register

Offset=0x0008

Bits	Name	Description	R/W	Reset
31:0	IODAT	GPIOA [31:0] Input/Output Data.	RW	0

25.3.4 GPIO_BOUTEN

GPIOB Output Enable Register

Offset=0x000c

Bits	Name	Description	R/W	Reset
31:0	OUTEN	GPIOB [31:0] Output Enable. 0: Disable 1: Enable	RW	0

25.3.5 GPIO_BINEN

GPIOB Input Enable Register

Offset=0x0010

Bits	Name	Description	R/W	Reset

31:0	INEN	GPIOB [31:0] Input Enable. 0: Disable 1: Enable	RW	0

25.3.6 GPIO_BDAT

GPIOB Data Register

Offset=0x0014

Bits	Name	Description	R/W	Reset
31:0	IODAT	GPIOA [31:0] Input/Output Data.	RW	0

25.3.7 GPIO_MFCTL2

Multi Function Control Register2

Offset=0x0020

Bits	Name	Description	R/W	Reset
31:21	-	Reserved	R	0
20	LDR_PWM1	LDR_PWM1 output enable and mapping to UART1TX. 0: disable 1: enable	RW	0
19	LDR_PWM0	LDR_PWM0 output enable and mapping to UART1RX. 0: disable 1: enable	RW	0
18	LDR_CONDRV	Pad driver control of LDR control signals (LDRDE;LDRDCLK;LDRHSYNC;LDRVSYNC): 0: normal driver 1: double driver If this bit is set, the corresponding pad's driver is enhanced according to LCD_CTENx.	RW	0
17	LDR_DATDRV	Pad driver control of LDR data signals: 0: normal driver 1: double driver If this bit is set, the corresponding pad's driver is enhanced according to LCD_CTENx.	RW	0
16:0	-	Reserved	RW	0

25.3.8 PAD_DRV

PAD Driver control Register

Offset=0x0088

Bits	Name	Description	R/W	Reset
31	U1RC	I2C1SCL & I2C1SDA 1: Double drive 0:normal drive	RW	0
30	U1RT	UART1RX & UART1TX 1: Double drive 0:normal drive	RW	0
29:27	-	Reserved	RW	0
26:24	KOUT	KSOUT[2:0] 0x7:Double drive 0x0:normal drive	RW	0
23:20	-	Reserved	RW	0
19:16	KIN	P_KSIN[3:0] 0xf: Double drive 0x0:normal drive	RW	0
15	-	Reserved	RW	1
14	DRDL	SDRDQ[15: 0] 1: Double drive 0:normal drive	RW	1
13	DRA	SDRA[12:0] 1: Double drive 0:normal drive	RW	1
12	DRBA	SDRBA[1:0] 1:Double drive 0:normal drive	RW	1
11	DRWE	SDRWEB 1: Double drive 0:normal drive	RW	1
10	DRCA	SDRCASB 1: Double drive 0:normal drive	RW	1
9	DRRA	SDRRASB 1:Double drive 0:normal drive	RW	1
8	DQM	SDRDQM[1:0] 1: Double drive 0:normal drive	RW	0
7	-	Reserved	RW	0
6	BT	BTD[7:0],BTVSYNC,BTHSYNC,BTPCLK,BTMCLK 1: Double drive 0:normal drive	RW	0
5:0	-	Reserved	RW	0

26 *Electrical Characteristics*

26.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply voltage	VDD	1.5	2.1	V
	VCC	2.8	3.4	V
Input voltage	VIH	2.8	3.4	V
	VIL		0.3	V
Junction Temperature	Tj		150	℃
Lead Temperature	(Soldering, 10 sec)		260	℃
Storage temperature	Tstg	-65	150	℃

Note:

1. TO = 25℃（Operating Temperature）, VDD = 1.8 V, VCC = 3.1 V
2. Do not short-circuit two or more output pins simultaneously.
3. Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.
4. The specifications and conditions shown in the DC and AC characteristics are the ranges for normal operation and the quality assurance of the product.

26.2 Capacitance

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Input capacitance	C_I	f_C = 1 MHz		20	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V		20	pF

Note: To = 25℃, VCC = 0 V.

26.3 DC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-level output voltage	V_{OH}	I_{OH} = -2 mA	2.4			V
Low-level output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
High-level input voltage	V_{IH}		0.9VCC		VCC+0.3	V
Low-level input voltage	V_{IL}		-0.3		0.1VCC	V
Input leakage current	I_{LI}	VCC = 3.6 V, VI = VCC, 0 V			+10	uA
Output leakage current	I_{LO}	VCC = 3.6 V, VI = VCC, 0 V			+5	uA

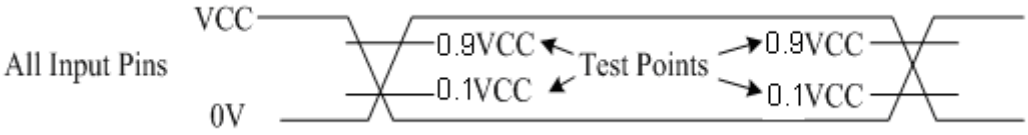
Notes:

1. TA = 0 to +70℃, VDD = 1.8 V, VCC = 3.1 V

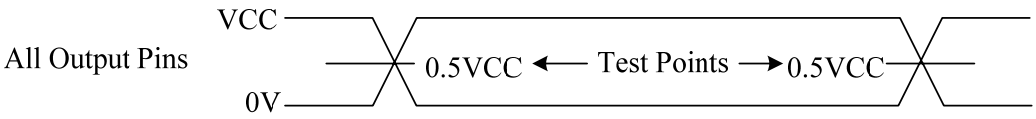
26.4 AC Characteristics

To = 0 to +70℃, VDD = 2 to 3 V, VCC = 2.7 to 3.6 V

26.4.1 AC Test Input Waveform

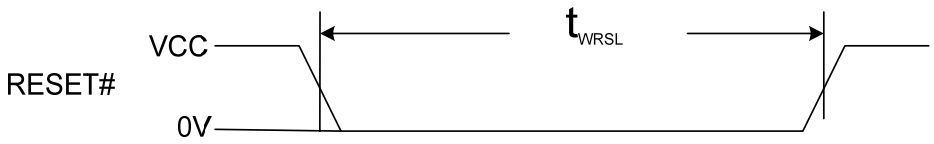


26.4.2 AC Test Output Measuring Points



26.5 Reset Parameter

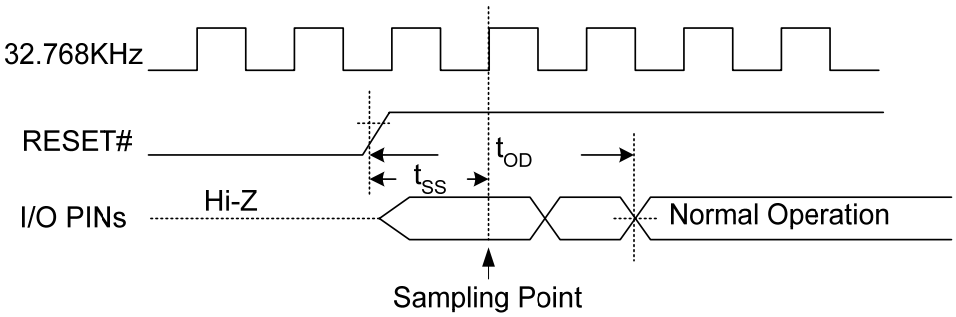
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Reset input low-level width	t_{WRSL}	RESET# pin	230		us



Reset Timing

26.6 Initialization Parameter

Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data sampling time (from RESET#)	t_{SS}			120	us
Output delay time (from RESET#)	t_{OD}			120	us



Initialization Timing

26.7 PMU

26.7.1 DC/DC Operates Voltage

In Li-ion mode, DC/DC operates with battery as low as 2.8V.

26.7.2 System Standby Dissipation

Parameter	MIN (uA)	Typical (uA)	MAX (uA)
IVCC+IAVCC		100	110
IVDD		40	55
IAVDD		3.5	4.5
RTCVDD		1.0[1]	
		0.3[2]	
IUVCC		12	15

Note1: When ex osc is enabled

Note2: When ex osc is disabled

26.7.3 Vccout Load Capability

Parameter	MIN(mA)	Typical(mA)	MAX(mA)
VCCOUT	50	100	

Note: the parameter is tested when VCC is 3.1V and VCCOUT is 95% VCC.

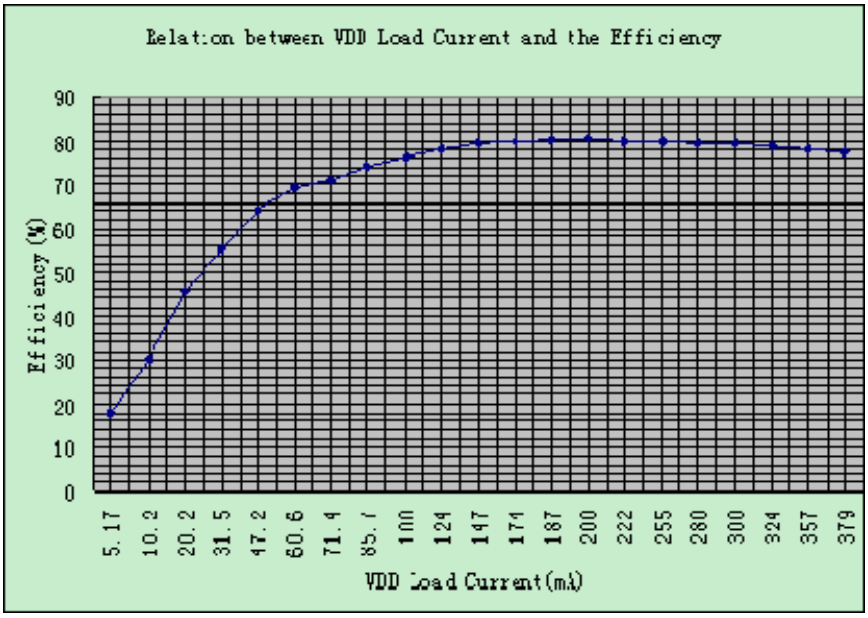
26.7.4 LRADC

ERROR / Parameter		MIN	TYPICAL	MAX	Unit
REMO_ADC		-	-	200	mV
BAT_ADC	Li-ION	-	-	50	mV

DC/DC Efficiency Curve

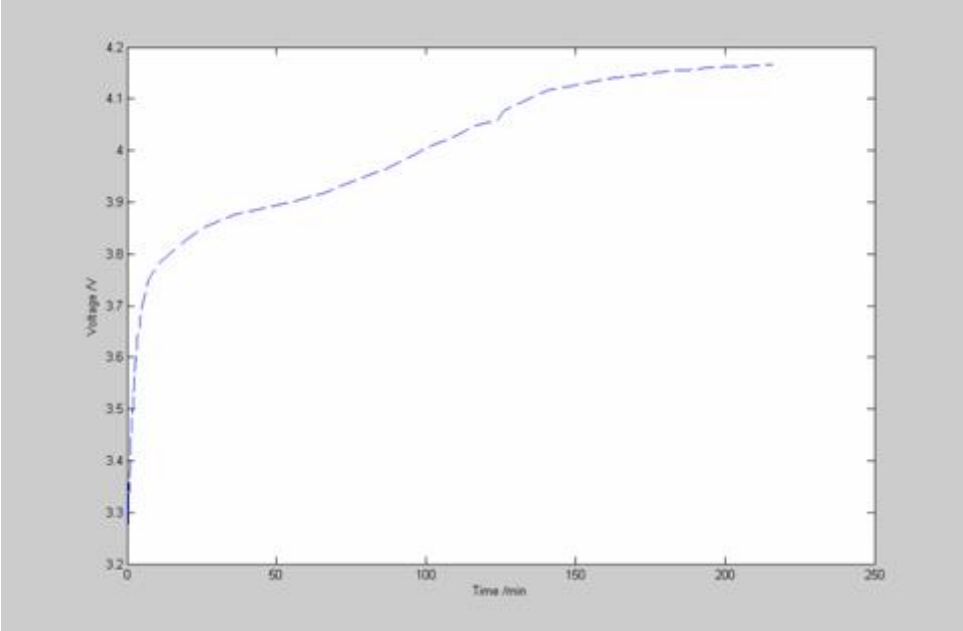
(Please refer to the corresponding schematic diagram of reference circuit for DC/DC circuit components parameter)

Li-ION, VBAT=3.6V



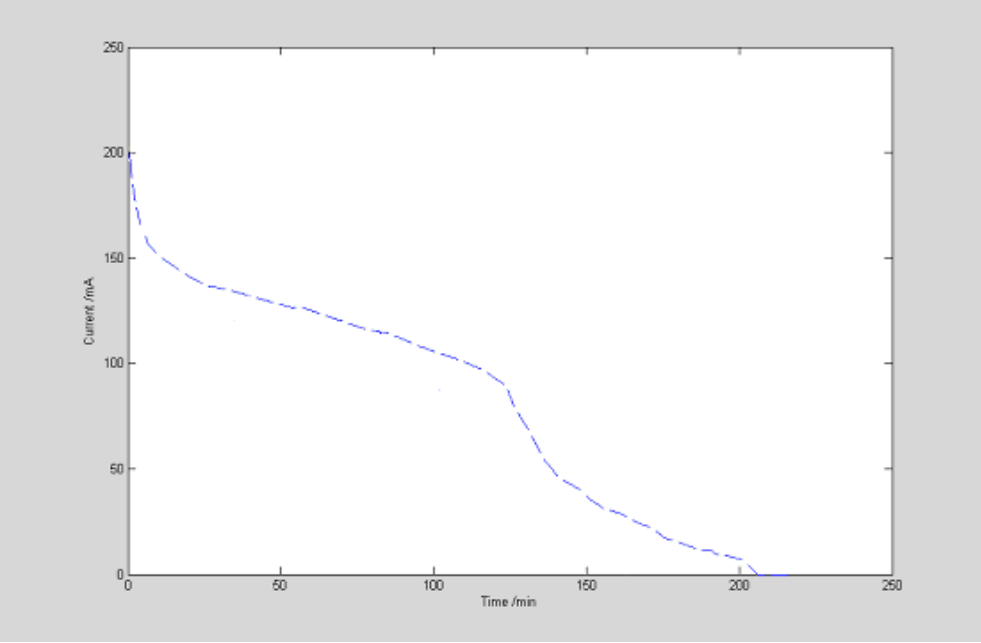
VDD Load Current-Efficiency Relation (Li-ION)

Charging Curve of the Charger—Voltage Characteristics Curve



Charging Curve of the Charger—Voltage Characteristics Curve

Charging Curve of the Charger—Current Characteristics Curve



Charging Curve of the Charger—Current Characteristics Curve

Note: the above results are measured when charging 270mAh Li-ion battery at the charging current of 200mA.

LDO Load Capacity

LDO Input	IVCC			IVDD		
	MIN (mA)	Typical (mA)	MAX (mA)	MIN (mA)	Typical (mA)	MAX (mA)
3.6V	320	350		350	400	
4.5V	350	380				
5.0V	420	480				

Note: the parameter is tested when VOUT is Drop 95%.

26.8 GPIO Interface Parameter

Parameter	Symbol	Condition	MIN.	TYPE	MAX.	Unit
GPIO output rise time	t_{GPRISE}		3		40	ns
GPIO output fall time	t_{GPFALL}		3		40	ns

Output timing:

GPIO Output Timing

Table: GPIO Drive

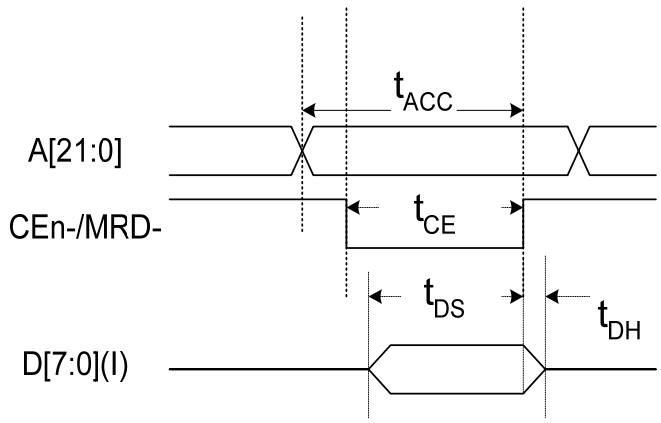
ATJ2259B (VCC=3.340V)				
GPIO_X	Pin_Name	IoH	IoL	Power up status (CEOS=1)
A31	SIRQ0	2mA	2mA	z
A30	LDRD19	8mA	8mA	0
A29	LDRD15	8mA	8mA	0
A28	LDRD14	8mA	8mA	addr-0
A27	LDRDCLK	8mA	8mA	0
A26	SDRA12	8mA	8mA	0(oen)
A25	SDRA11	8mA	8mA	0(oen)
A24	LDRD11	8mA	8mA	data-0(oen)

A23	LDRD10	8mA	8mA	data-0(oen)
A22	LDRD13	8mA	8mA	data-1(oen)
A21	LDRHSYNC	8mA	8mA	data-1(oen)
A20	LDRVSYNC	8mA	8mA	data-0(oen)
A19	LDRD21	8mA	8mA	data-0(oen)
A18	LDRD12	8mA	8mA	data-1(oen)
A17	NF_CEB2	16mA	16mA	1
A16	NF_RB2	8mA	8mA	1
A15	DRVVBUS	8mA	8mA	0
A14	LDRD23	8mA	8mA	0
A13	KSOUT1	2mA	2mA	z
A12	KSOUT0	2mA	2mA	z
A11	KSIN3	2mA	2mA	z
A10	KSIN2	2mA	2mA	1
A9	KSIN1	2mA	2mA	1
A8	KSIN0	2mA	2mA	1
A7	I2C1SDA	8mA	8mA	z
A6	I2C1SCL	8mA	8mA	z
A5	LDRD5	8mA	8mA	0
A4	LDRD4	8mA	8mA	0
A3	LDRD3	8mA	8mA	0
A2	NF_CLE	8mA	8mA	addr-0
A1	NF_RB	8mA	8mA	addr-0
A0	NF_ALE	8mA	8mA	ale-0
GPIO_X		IoH	IoL	**Power up status (CE0S=1)**
B31	SIRQ1	2mA	2mA	z
B30	LDRD20	8mA	8mA	0
B29	SD_CLK	16mA	16mA	1-sdclk-1
B28	NF_CEB3	8mA	8mA	1
B27	NF_CEB0	8mA	8mA	ce-1
B26	GPIOB26	16mA	16mA	Z
B22	KSOUT2	2mA	2mA	1

B17	LDRD22	8mA	8mA	z
B16	GPIOB16	8mA	8mA	0
B15	UART1RX	8mA	8mA	z
B14	UART1TX	8mA	8mA	1
B11	BTMCLK	8mA	8mA	0
B10	BTVSYNC	8mA	8mA	0
B9	BTHSYNC	8mA	8mA	0
B8	BTPCLK	8mA	8mA	0
B7	BTD7	8mA	8mA	0
B6	BTD6	8mA	8mA	0
B5	BTD5	8mA	8mA	0
B4	BTD4	8mA	8mA	0
B3	BTD3	8mA	8mA	0
B2	BTD2	8mA	8mA	0
B1	BTD1	8mA	8mA	0
B0	BTD0	8mA	8mA	0

26.9 Ordinary ROM Parameter

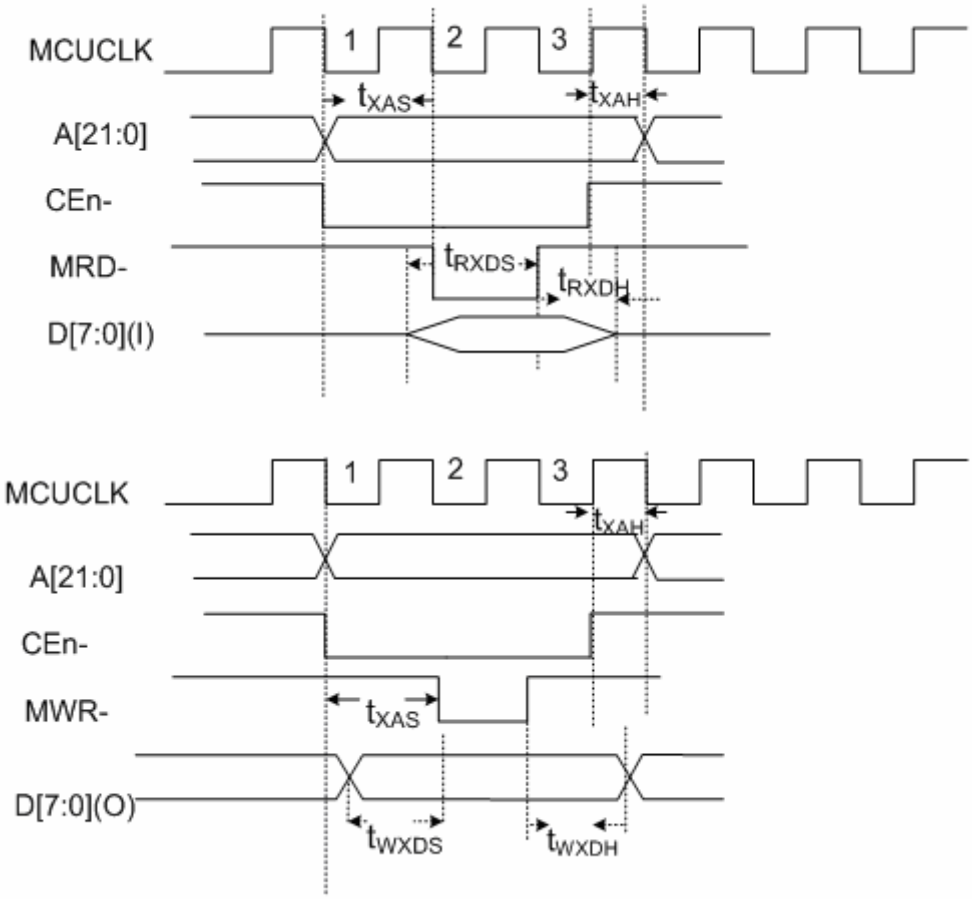
Parameter	Symbol	Condition	MIN.	MAX.	Unit
Data access time (from address)Note	t_{ACC}	HOSC=24MHz	102		ns
Data access time (from CEx#)Note	t_{CE}	HOSC=24MHz	82		ns
Data input setup time	t_{DS}	HOSC=24MHz	5		ns
Data input hold time	t_{DH}	HOSC=24MHz	5		ns



Ordinary ROM Timing

26.10 External System Bus Parameter

External System Bus Timing



External System Bus Parameter

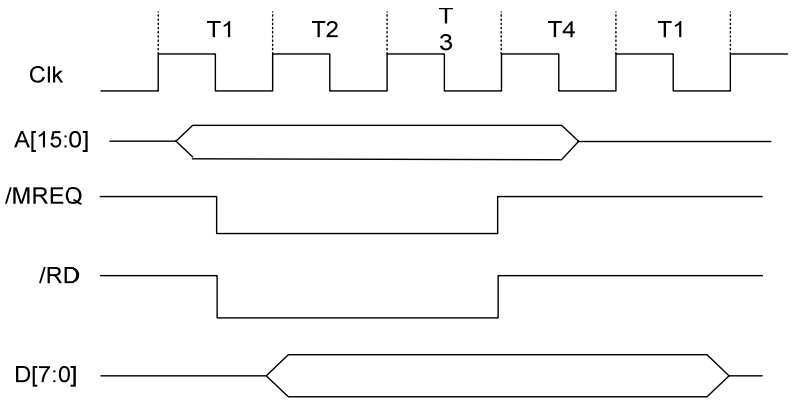
Parameter	Symbol	Condition	MIN.	MAX	Unit
Address setup time (to command signal)Note 1, 2	t_{XAS}	Memory Read	25		ns
	t_{XAS}	Memory Write	10		ns
Address hold time (from command signal)Note 1, 2	t_{XAH}		5		ns
Data output setup time (to command signal)Note 1	t_{WXDS}		20		ns
Data output hold time(from command signal)Note 1	t_{WXDH}		10		ns
Data input setup time (to command signal)Note 1	t_{RXDS}		20		ns

Data input hold time (from command signal)Note 1	t_{RXDH}		10		ns

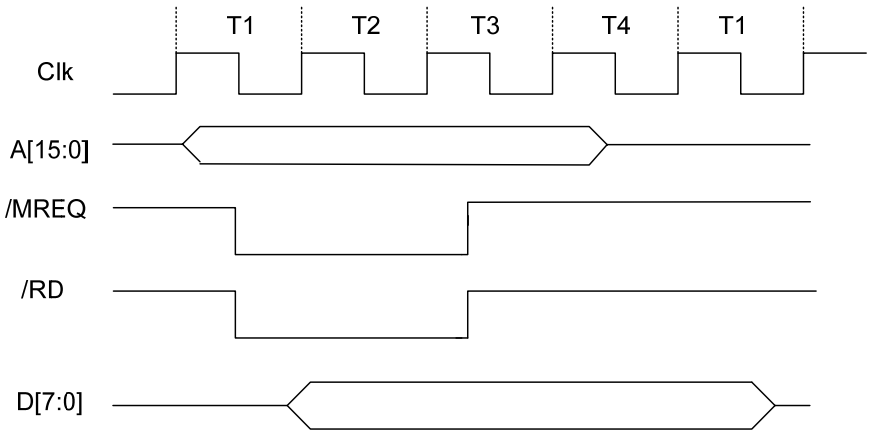
Notes:

1. MRD#, MWR# are called the command signals for the External System Bus Interface.
2. T (ns) = 1/ f_{MCUCLK}

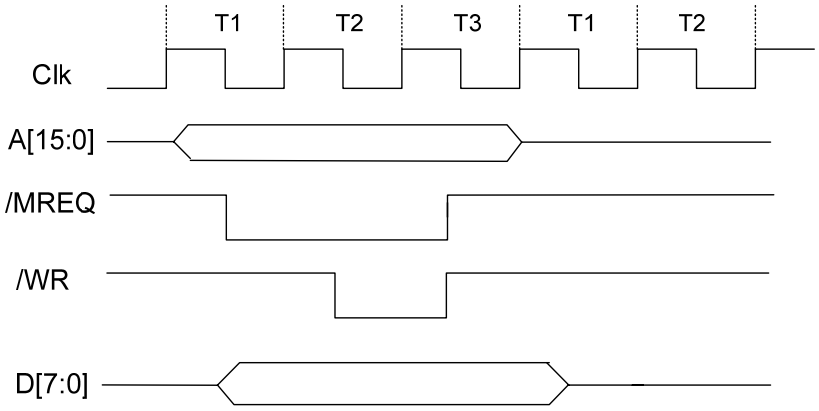
26.11 Bus Operation



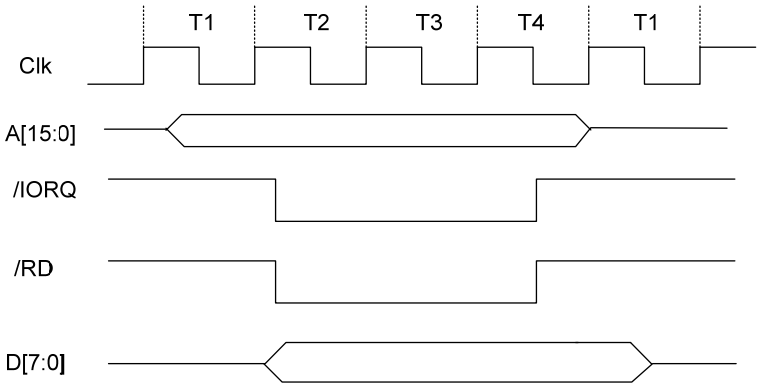
Instruction Fetch Timing



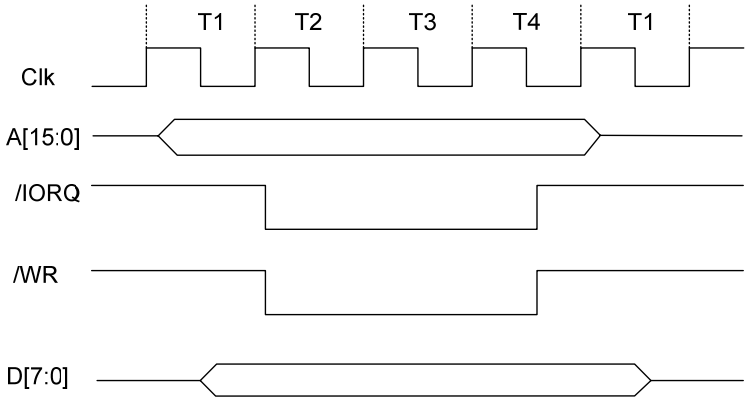
Memory Read Timing



Memory Write Timing

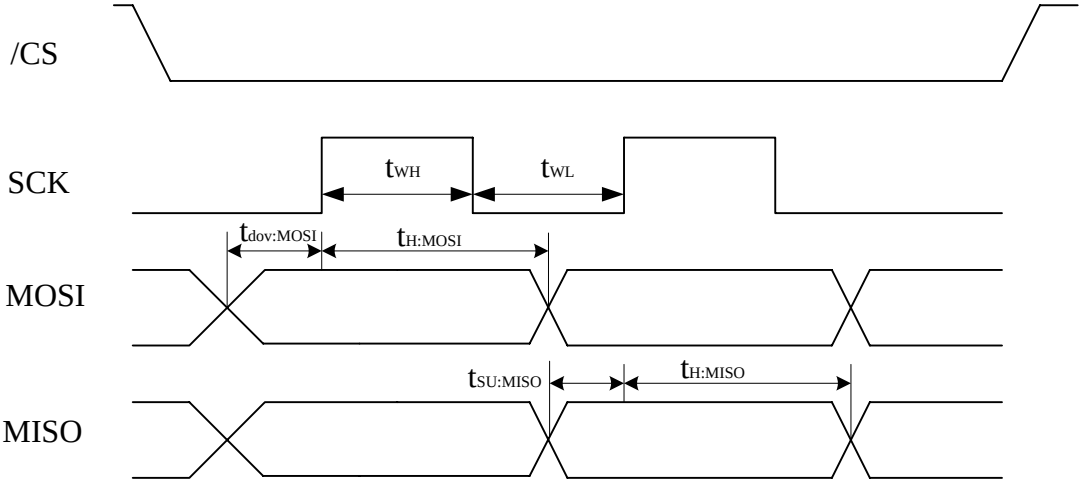


IO Read Timing



IO Write Timing

26.12 SPI Parameter



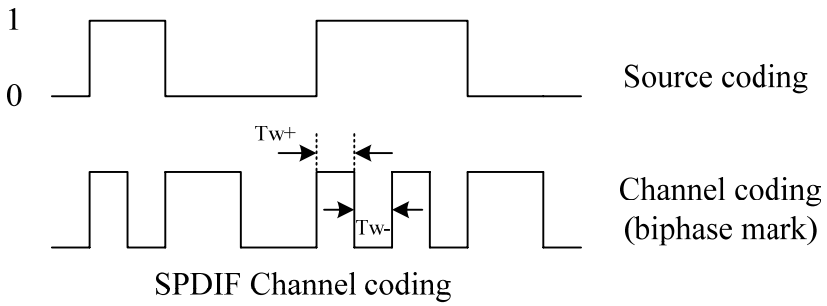
SPI timing

CoreCLK=180M, Sclk=90M, PCLK=45M, CLKDIV=3, SPICLK=7.5M, double the drive ability at PAD_DRV.

SPI Parameter

Parameter	Symbol	Min	Max	Unit
SCK Clock	fclk		7.5	MHz
SCK High time	t_{WH}	66		ns
SCK Low time	t_{WL}	68		ns
SCK rise time	t_r		11.6	ns
SCK fall time	t_f		12.8	ns
Data output valid	$t_{DOV:MOSI}$	14		ns
Data output hold	$t_{H:MOSI}$	100		ns
Data in setup time	$t_{SU:MISO}$	14		ns
Data in hold time	$t_{H:MISO}$	100		ns

26.13 SPDIF Interface Parameter



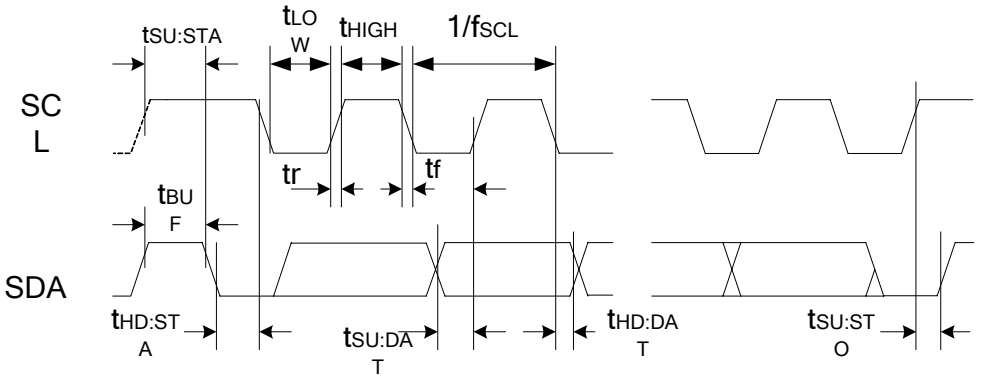
SPDIF Channel Coding

Sampling Rate	Channel Bit Theoretical Value	Channel Bit Tw+	Channel Bit Tw-
32K	244nS	242nS	246
44.1K	177nS	176nS	178
48K	163nS	161nS	163

26.14 I2C Interface Parameter

Parameter	Symbol	Typical		Unit
SCL period	f_{SCL}	100	400	kHz
Clock low time	T_{LOW}	5.0	1.26	us
Clock high time	T_{HIGH}	4.96	1.22	us
Clock rise time	t_r	90	90	ns
Clock fall time	t_f	7.5	8	ns
Data setup time	$t_{SU:DAT}$	3.7	0.68	us
Data hold time	$t_{HD:DAT}$	1.24	0.74	us
Start hold time	$t_{HD:STA}$	9.2	2.45	us
Start setup time	$t_{SU:STA}$	5.3	1.3	us
Stop setup time	$t_{SU:STO}$	5.3	1.3	us

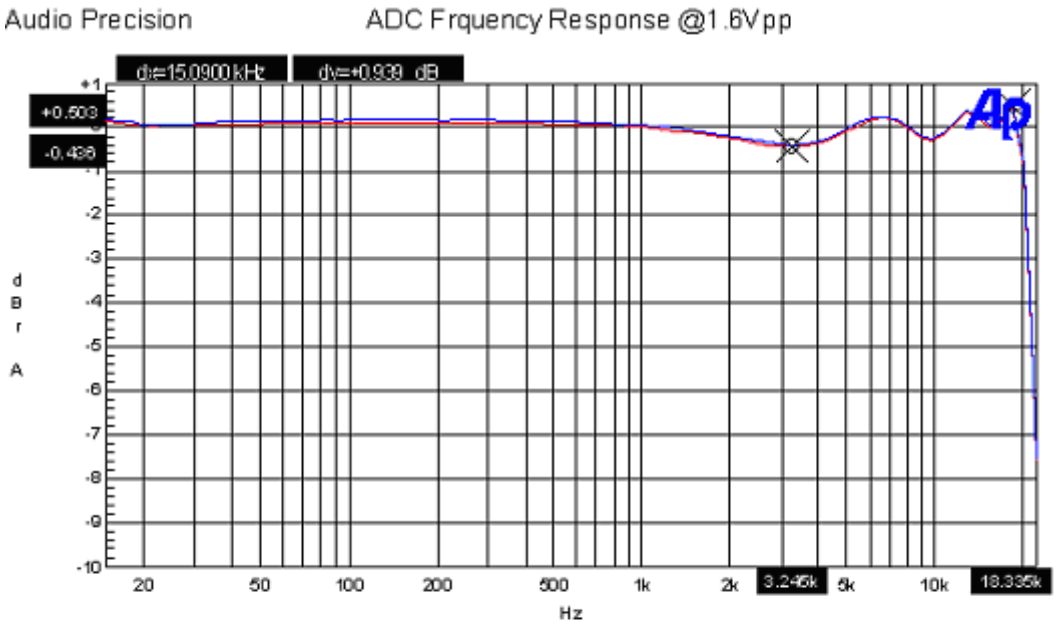
I2C Interface Timing



26.15 A/D Converter Characteristics

(TA = -10 - +70℃, VDD = 1.6 V, VCC = 3.1V, AVCC = 2.9V, Sample Rate=48 KHz)

Characteristics	Min.	Typical	Max.	Unit
Dynamic Range –40 dBFS Input		85.5		dB
Total Harmonic Distortion+Noise		-82.0		dB
Frequency Response 20-18KHz	-0.4		0.5	dB
Reference Voltage		1.502/1.502		V
Full Scale Input Voltage		2.81		Vpp



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Red	Solid	1	Anlr.Level A	Left		*-0.436 dBr A	*+0.503 dBr A
1	2	Blue	Solid	1	Anlr.Level B	Left		-0.389 dBr A	+0.549 dBr A

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

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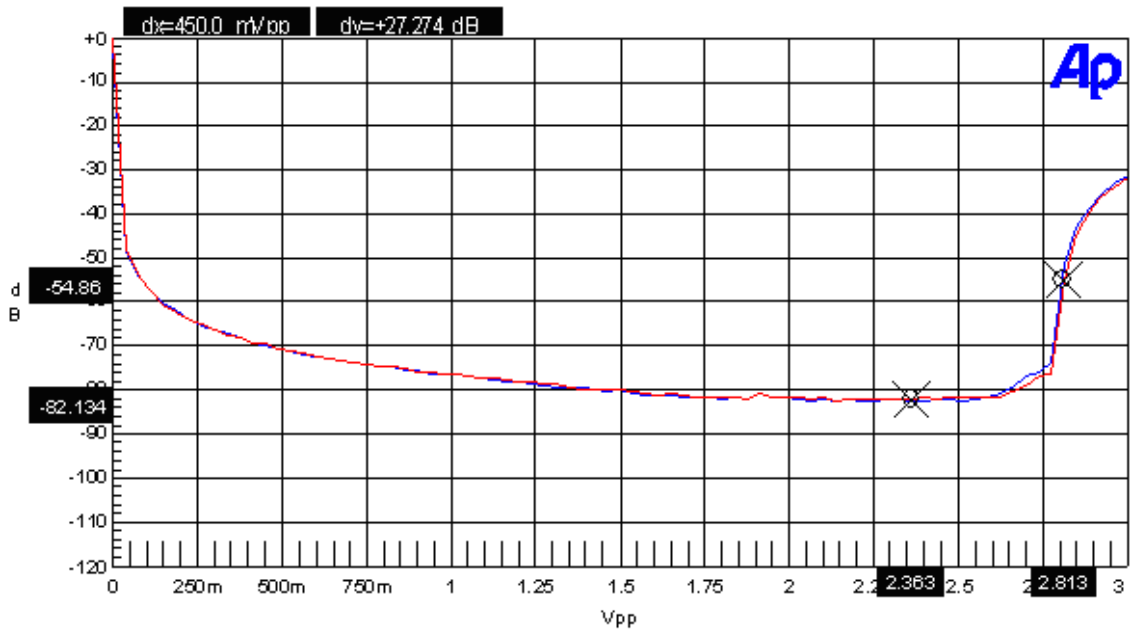
ADC Frequency Response



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Red	Solid	1	Anlr.THD+N Ratio	Left		*-82.134 dB	*-54.860 dB
1	2	Blue	Solid	1	Anlr.THD+N Ratio	Left		-82.361 dB	-51.535 dB

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

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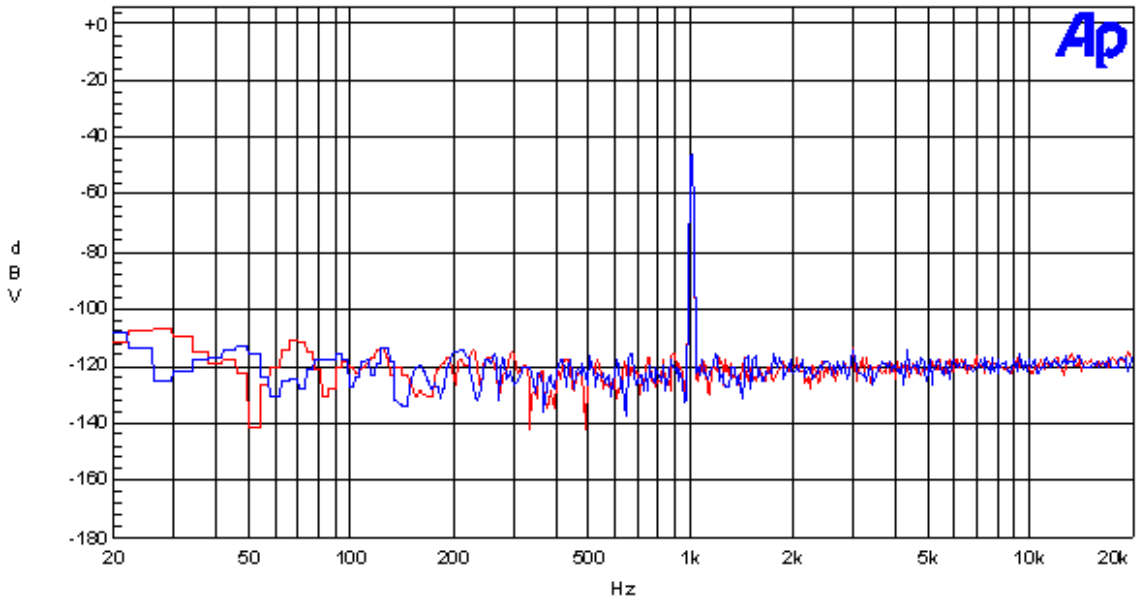
ADC thd vs Amplitude

Audio Precision ADC FFT @1kHz,-40dBFS,48kSR



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Fft Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft Ch.2 Ampl	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

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ADC Small Signal Power Spectrum

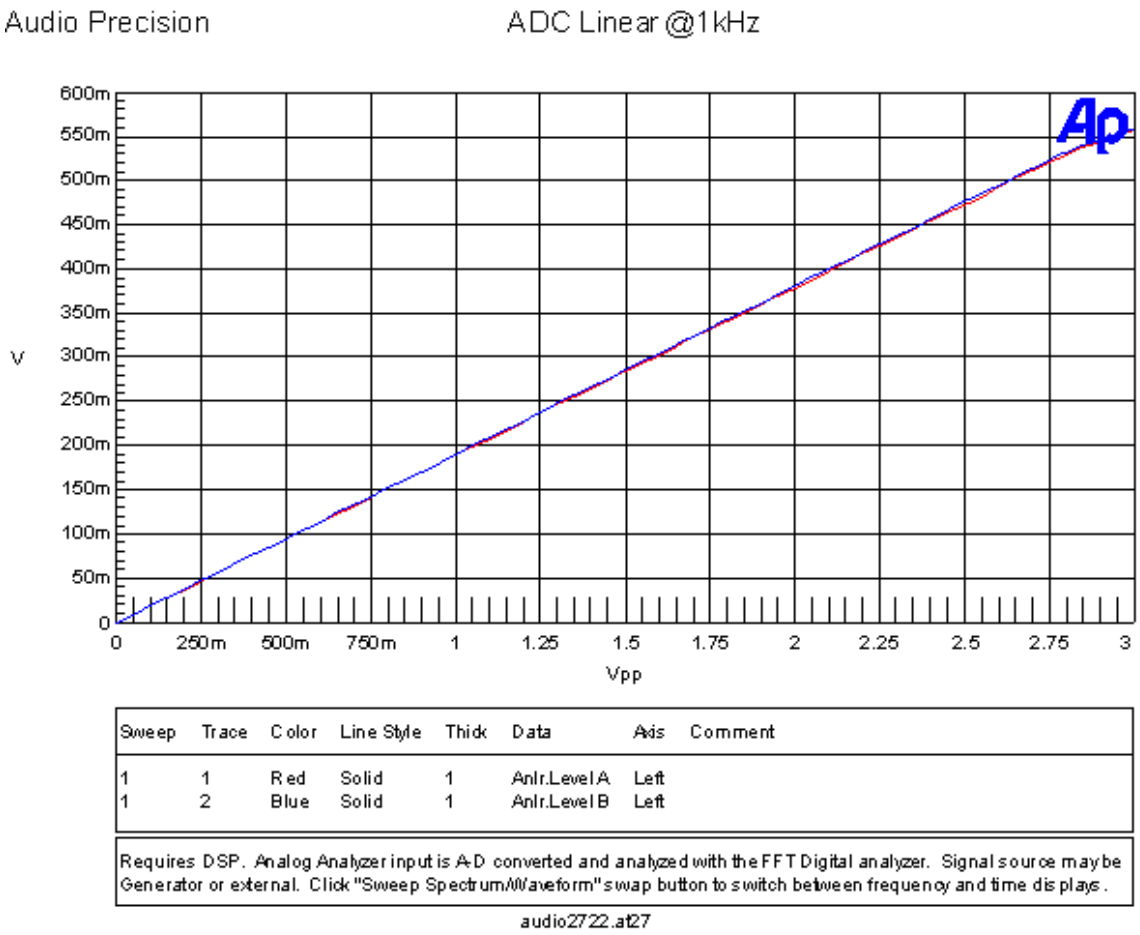


Figure: ADC Linearity

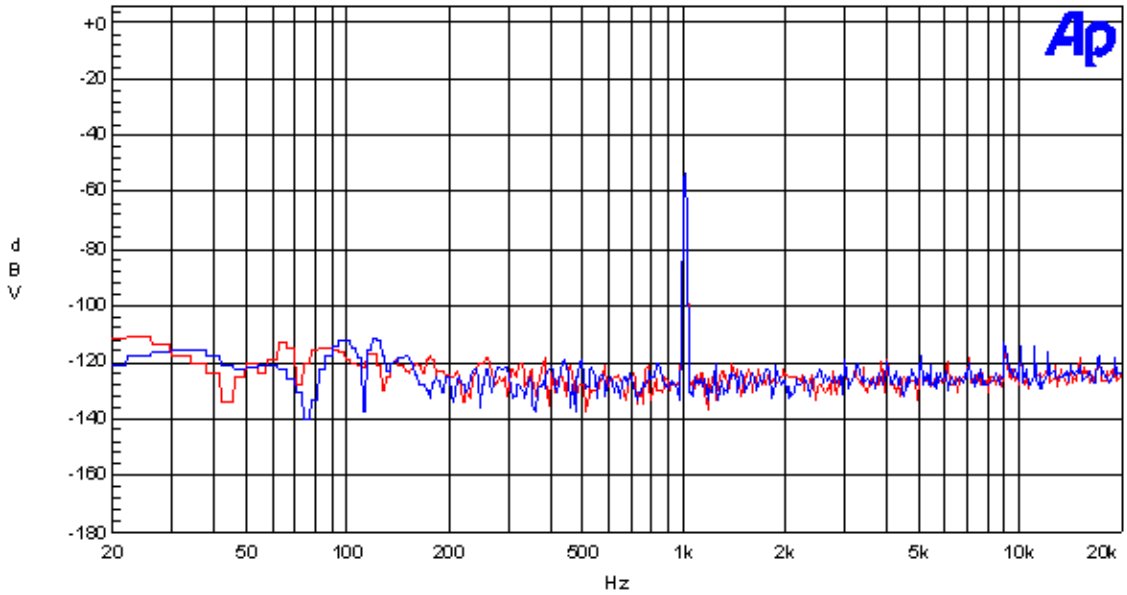
26.16 D/A Converter Characteristics

D/A Converter Characteristics

(TA = -10 - +70℃, VDD = 1.6 V, VCC = 3.1V, AVCC = 2.9V, Sample Rate=48 KHz)

Characteristics	Min.	Typical	Max.	Unit
Dynamic Range –48 dBFS Input		91.0		dB
Total Harmonic Distortion+Noise		-83.0		dB
Full Scale Output Voltage	0.48	0.58	0.72	Vrms
Interchannel Isolation (1k)		-108/-78.5		dB

Audio Precision DAC+PA FFT @1kHz,-48dBFS,16.5R



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Fft.Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft.Ch.2 Ampl	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

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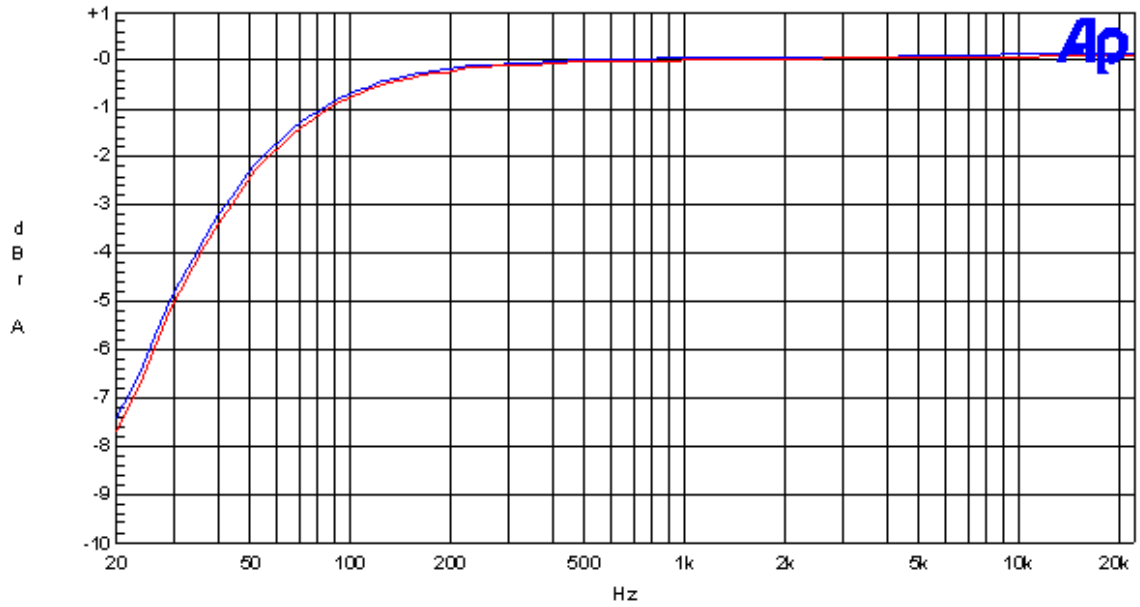
Figure: DAC Small Signal Frequency Spectrum

26.17 Headphone Driver Characteristics

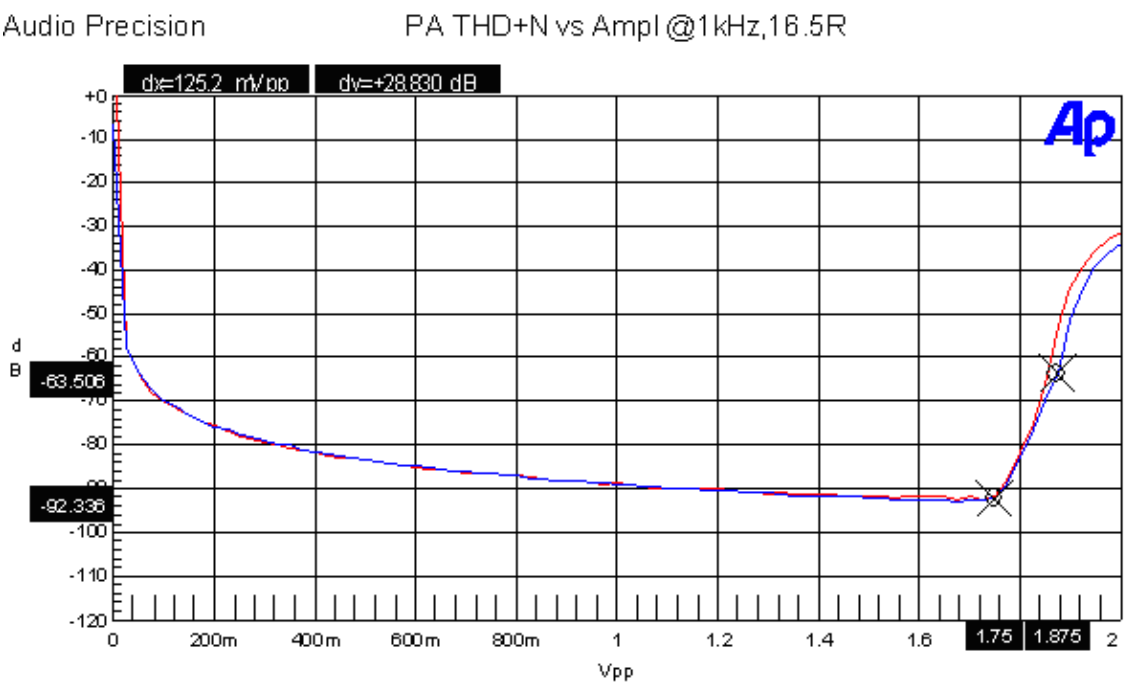
Headphone Driver Characteristics

(TA =-10 - +70℃, VDD = 1.6 V, VCC = 3.1V, AVCC = 2.9V Sample Rate=48 KHz, Volume Level=0x1F, 16.5ohms)

Characteristics	Min.	Typical	Max.	Unit
Dynamic Range		95.0		dB
Total Harmonic Distortion+Noise		-92.0		dB
Output Common Mode Voltage		1.515/1.515		Vrms
Full Scale Output Voltage@-60dB thd+n		0.64		Vrms
Output Power @16ohm		24		mW



Frequency Response Diagram of Headphone Driver



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment	Cursor1	Cursor2
1	1	Red	Solid	1	Anlr.THD+N Ratio	Left		-91.801 dB	-52.440 dB
1	2	Blue	Solid	1	Anlr.THD+N Ratio	Left		*-92.336 dB	*-63.506 dB

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

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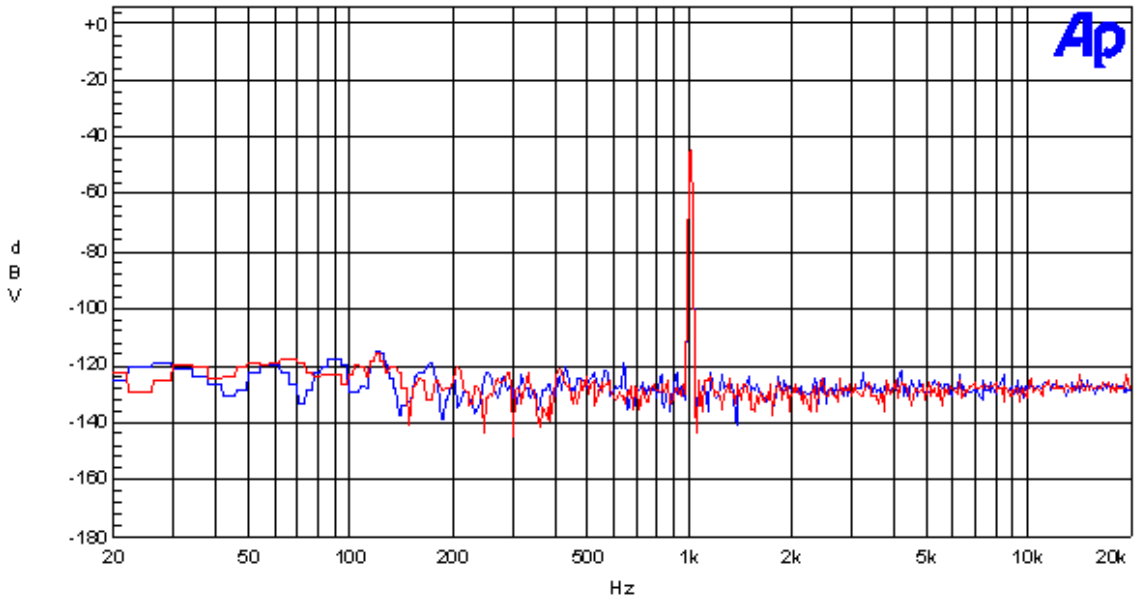
THD + N Amplitude Diagram of Headphone Driver

Audio Precision PA FFT @1kHz,-40dBFS,16.5R



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Fft Ch.1 Ampl	Left	
1	2	Blue	Solid	1	Fft Ch.2 Ampl	Left	

Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

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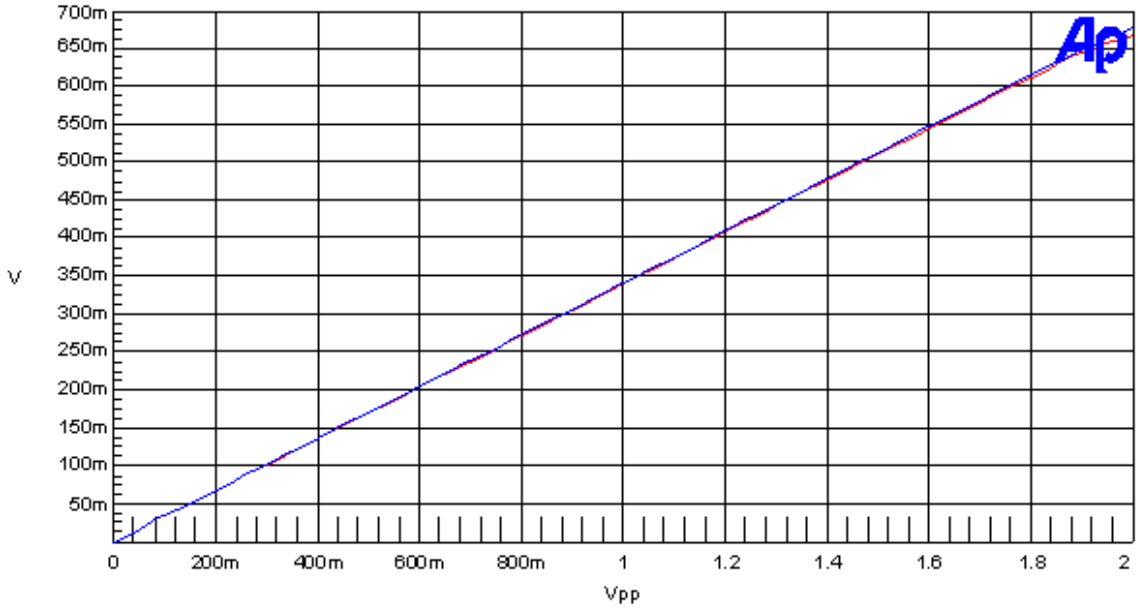
Small signal power spectrum of Headphone Driver

Audio Precision PA Linear@1kHz,16.5R



Sweep	Trace	Color	Line Style	Thick	Data	Axis	Comment
1	1	Red	Solid	1	Anlr.Level A	Left	
1	2	Blue	Solid	1	Anlr.Level B	Left	

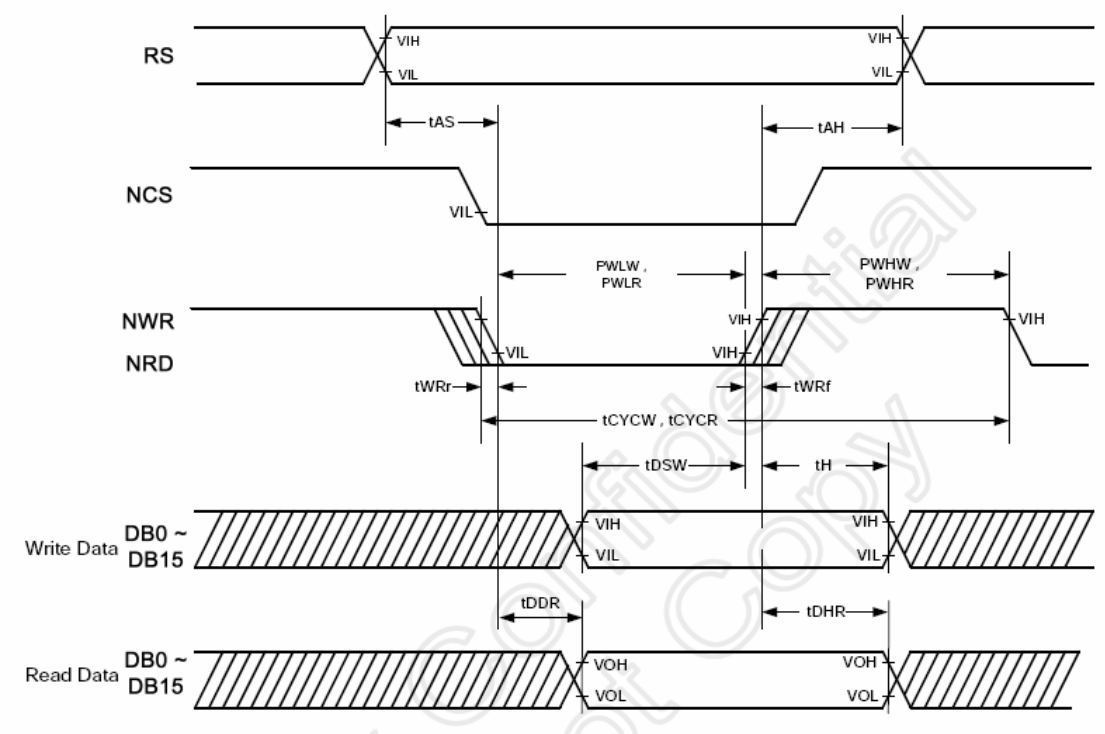
Requires DSP. Analog Analyzer input is A-D converted and analyzed with the FFT Digital analyzer. Signal source may be Generator or external. Click "Sweep Spectrum/Waveform" swap button to switch between frequency and time displays.

audio2722.at27

Linearity of Headphone Driver

26.18 LCM Driver Parameter

26.18.1 LDC LCM Driver Parameter



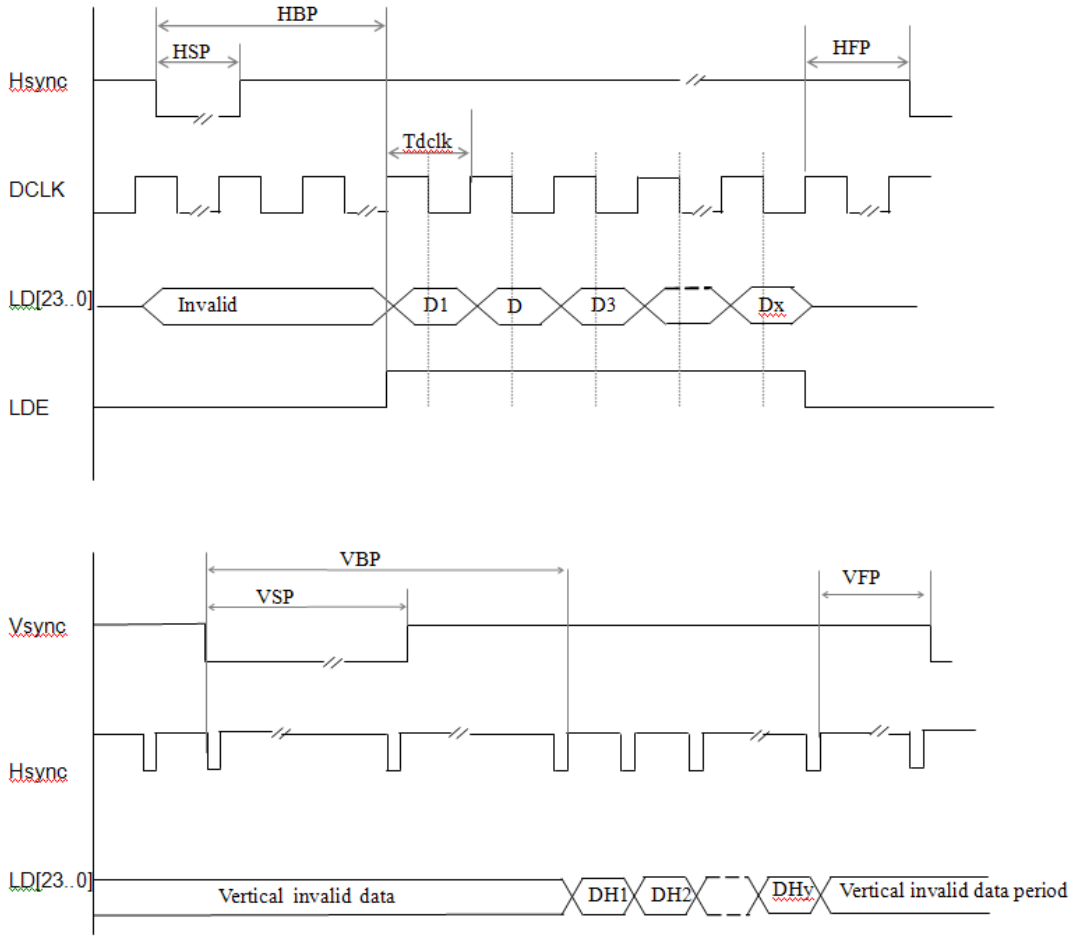
LCM Timing

LCM Driver Parameter

Item		Symbol	Unit	Min.	Typ.	Max.	Test Condition
Bus cycle time	Write	tCYCW	ns	34	200	-	AHB clk.=60MHz
	Read	tCYCR	ns	34	134	-	AHB clk.=60MHz
Write low-level pulse width		PWLW	ns	17	100	-	AHB clk.=60MHz
Read low-level pulse width		PWLR	ns	17	67	-	AHB clk.=60MHz
Write high-level pulse width		PWHW	ns	17	100	-	AHB clk.=60MHz
Read high-level pulse width		PWHR	ns	17	67	-	AHB clk.=60MHz
Write / Read rise / fall time		tWRr , tWRf	ns	-	11	-	AHB clk.=60MHz
Write data set up time		tDSW	ns	27	110	-	AHB clk.=60MHz
Write data hold time		tH	ns	23	28	-	AHB clk.=60MHz
Read data delay time		tDDR	ns	-	45	-	AHB clk.=60MHz

Read data hold time	tDHR	ns	-	105	-	AHB clk.=60MHz

26.18.2 LDR LCM Driver Parameter



LDR Parallel Mode Timing

LDR Serial Mode Timing:

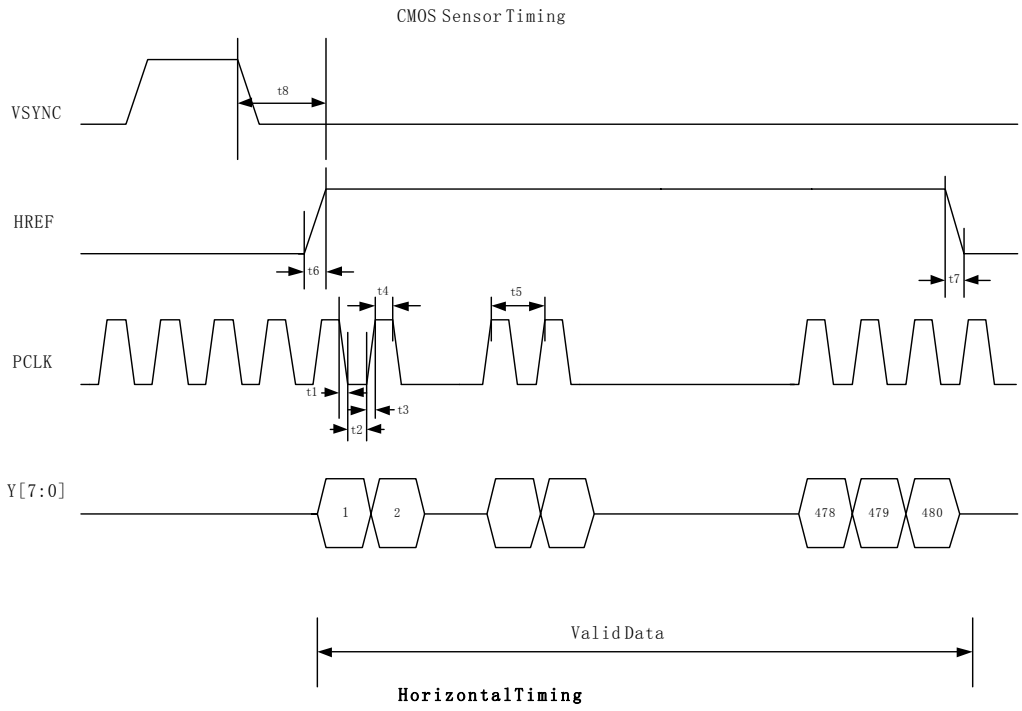
Make a reference to the "Parallel Mode Timing". The only difference between them is: when in serial mode, the RED,GREEN and BLUE ingredients of each pixel should be transmitted in serial (for example, 1st phase R[7..0], 2nd phase G[7..0], 3rd phase B[7..0], so the DCLK frequency will be triple as it's in parallel mode.)

LDR Driver Parameter (AT043TN13, 480x272 RGB Panel)

Item	Symbol	Unit	Min.	Typ.	Max.
Clock Cycle	$1/T_{dclk}$	MHz	-	9.00	15

Horizontal Front porch	HFP	CLK	2	-	-
Horizontal Pulse width	HSP	CLK	2	41	-
Horizontal Back porch	HBP	CLK	4	-	-
Vertical Front porch	VFP	H	2	2	-
Vertical Pulse width	VPW	H	2	10	-
Vertical Back porch	VBP	H	4	4	-
LDE Setup Time	t_{ldes}	ns	10	-	-
LDE Hold Time	t_{ldeh}	ns	10	-	-
Hsync Setup Time	t_{hs}	ns	10	-	-
Hsync Hold Time	t_{hh}	ns	10	-	-
Vsync Setup Time	t_{vhs}	ns	10	-	-
Vsync Hold Time	t_{vhh}	ns	10	-	-

26.19 CMOS Sensor Timing (same with BT601)

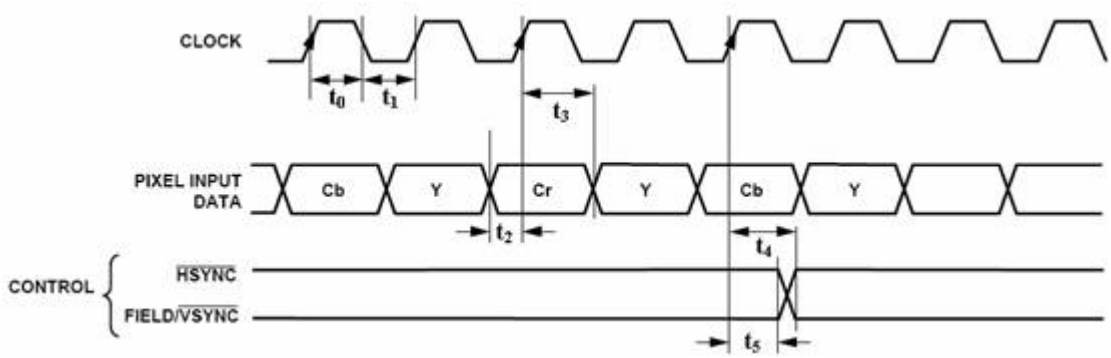


CMOS Sensor Timing

26.20 Encoder IF

Encoder IF Parameter

Parameter	Condition	Min	Typ	Max	Unit
clock	VCC=3.3V, VDD=1.6V		27		MHz
Clock High Time（t_0）			19		ns
Clock Low Time（t_1）			19		ns
Data Setup Time（t_2）			6		ns
Data Hold Time（t_3）			8		ns
Digital Output Access Time（t_4）			12		ns
Digital Output Hold Time（t_5）			8		ns

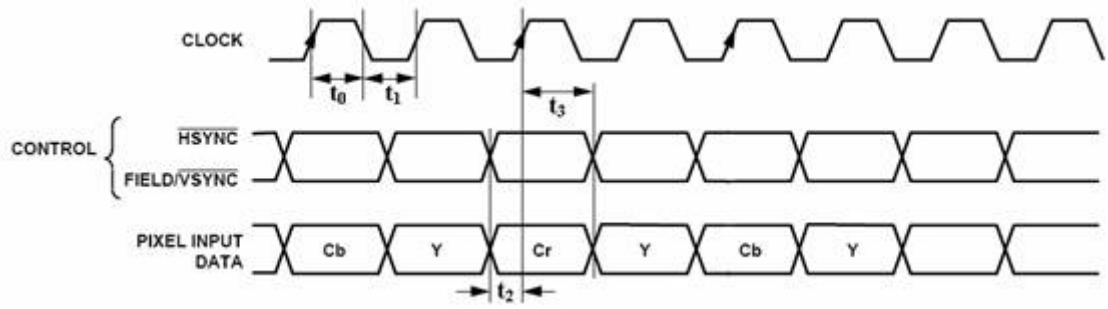


Encoder IF Timing

26.21 Decoder IF (BT656, BT601)

Decoder IF Parameter

Parameter	Condition	Min	Typ	Max	Unit
PCLK	VCC=3.3V, VDD=1.6V		27		MHz
Clock High Time（t_0）		8			ns
Clock Low Time（t_1）		8			ns
Data Setup Time（t_2）		3.5			ns
Data Hold Time（t_3）		4			ns



Decoder IF Timing

26.22 NAND Flash IF

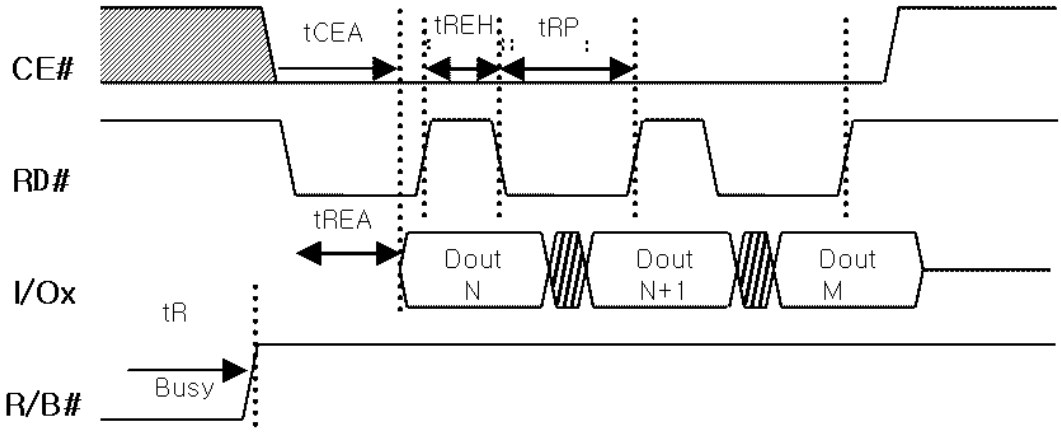


Figure: Data Fetch at RD# Rising Edge (Conventional Serial Access Mode)

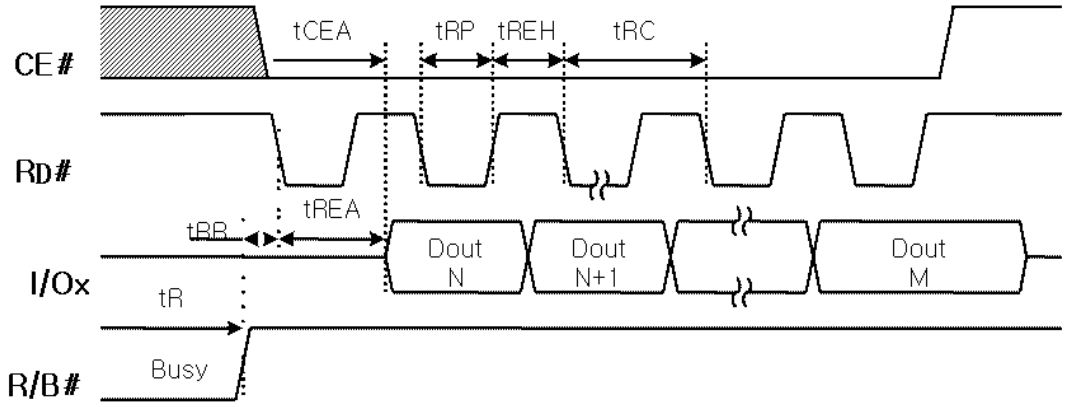


Figure: Data Fetch at RD# Falling Edge (EDO Type Serial Access Mode)

Command Latch Cycle

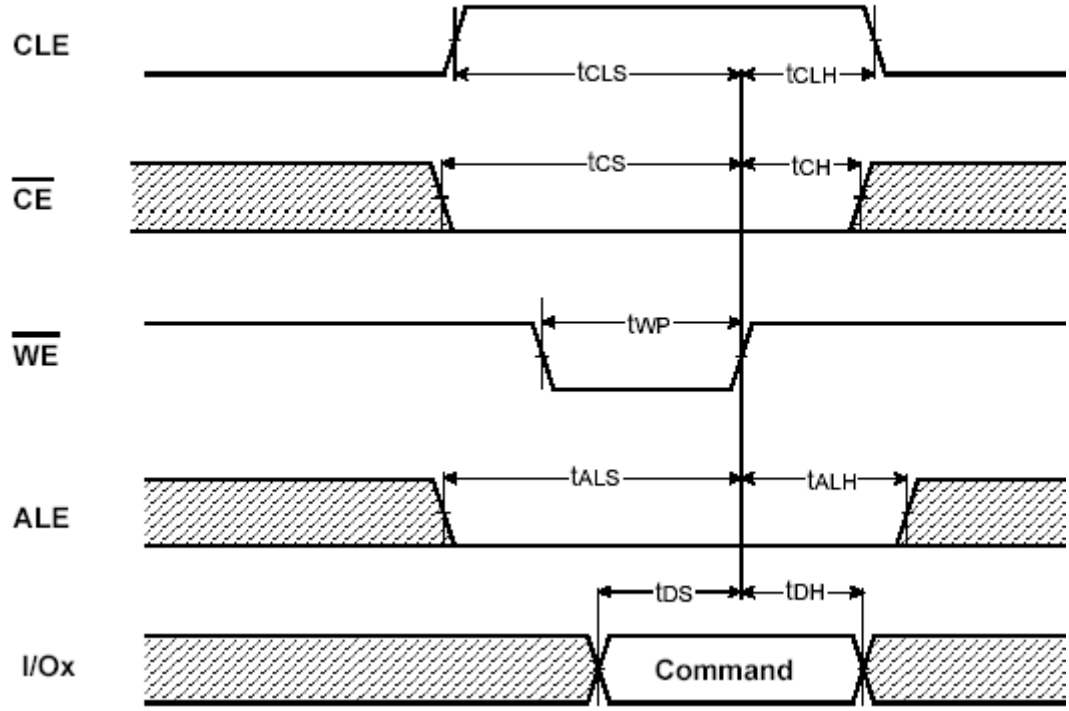
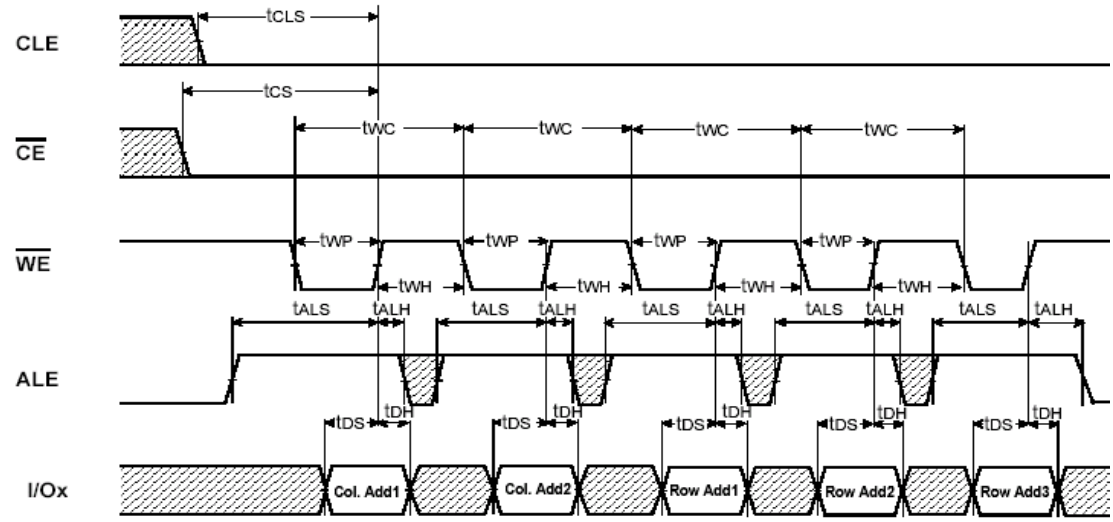


Figure: Command Latch Cycle
IO [15:8] must be set as zero

Address Latch Cycle



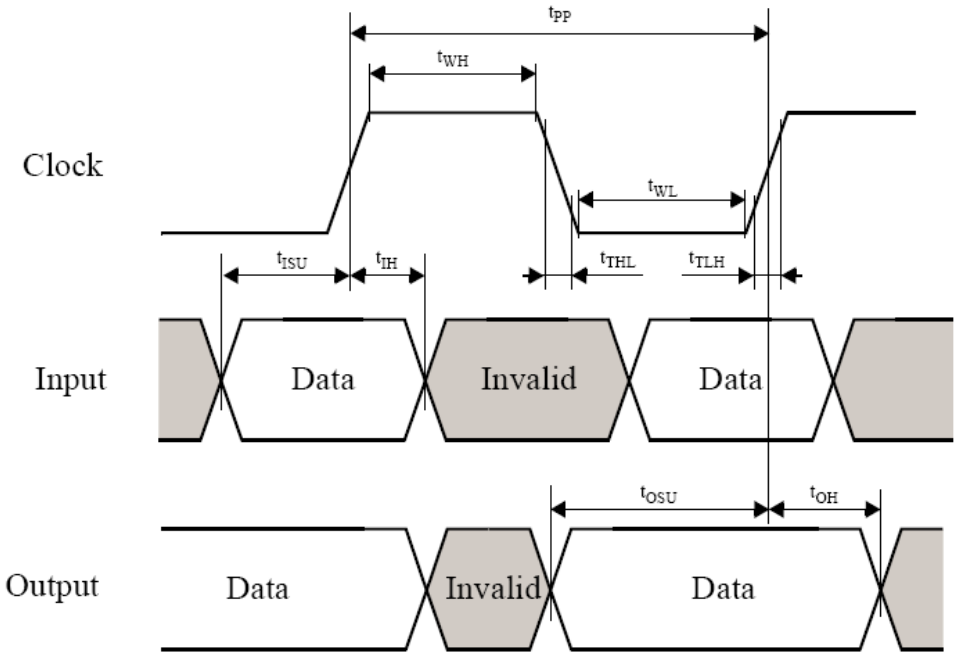
Address Latch Cycle
IO [15:8] must be set as zero

NAND Flash Interface Timing Reques

Item	Conventional	EDO type Serial Access	Remark

	Serial Access		
tCEA	23nS(min)	23nS(min)	
tREA	30nS(max)	18nS(max)	
tREH	15nS(min)	12.5nS(min)	
tRP	25nS(min)	12.5nS(min)	
tRC	30nS(min)	25nS(min)	Conventional: duty≠50% EDO type: duty=50%
Data Fetch	At RD# Rising Edge	At next RD# Falling Edge	
tFALLING	5nS	5nS	
tRISINFG	5nS	5nS	
tCLS	25nS(min)	12nS(min)	
tCLH	10nS(min)	5nS(min)	
tCS	35nS(min)	20nS(min)	
tCH	10nS(min)	5nS(min)	
tALS	25nS(min)	12nS(min)	
tALH	10nS(min)	5nS(min)	
tDS	20nS(min)	12nS(min)	
tDH	10nS(min)	5nS(min)	
tWC	30nS(min)	25nS(min)	
DMA clk	30MHz	40MHz	

26.23 SD/MMC IF



Timing Diagram Data Input/Output Referenced to Clock

SD Card Timing

Parameter	symbol	Min	Max	unit	Remark
Clock CLK					
Clock frequency data Transfer Mode (Push Pull)	fpp	0	26/52	MHz	CL<=30pF(tolerance +100KHz)
Clock frequency identification Mode(Open Drain)	fOD	0	400	KHz	Tolerance:+20KHz
Clock low time	tWL	6.5		ns	CL<=30pF
Clock rise time	tTLH		3	ns	CL<=30pF
Clock fall time			3	ns	CL<=30pF
Inputs CMD DAT(reference to CLK)					
Input setup time	tISU	3		ns	CL<=30pF
Input hold time	tIH	3		ns	CL<=30pF
Output CMD DAT(reference to CLK)					
Output setup time	tOSU	5		ns	CL<=30pF
Output hold time	tOH	5		ns	CL<=30pF
Signal rise time	trise		3	ns	CL<=30pF

Signal fall time	tfall		3	ns	CL<=30pF

Bus signal Line Load

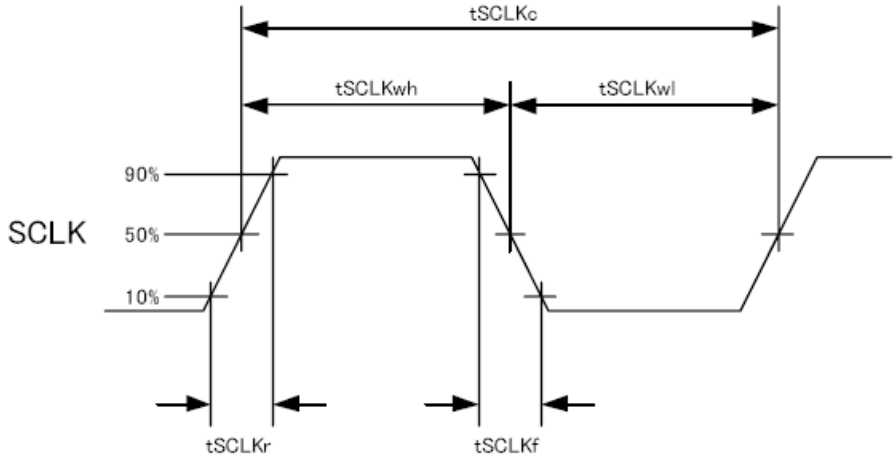
Parameter	Symbol	Min	Recommend	Max	Unit	Remark
Pull up resistance for CMD	Rcmd	4.7	10	100	KOhm	To prevent bus floating
Pull up resistance for dat0-7	Rdat	50	50	100	KOhm	To prevent bus floating
Bus signal line capacitance	CL			30	pF	Single card
Signal card capacitance	Ccard			7	pF	
Maximum signal line inductance				16	nH	Fpp<=52MHz

CL=CHost+Cbus+Ccard

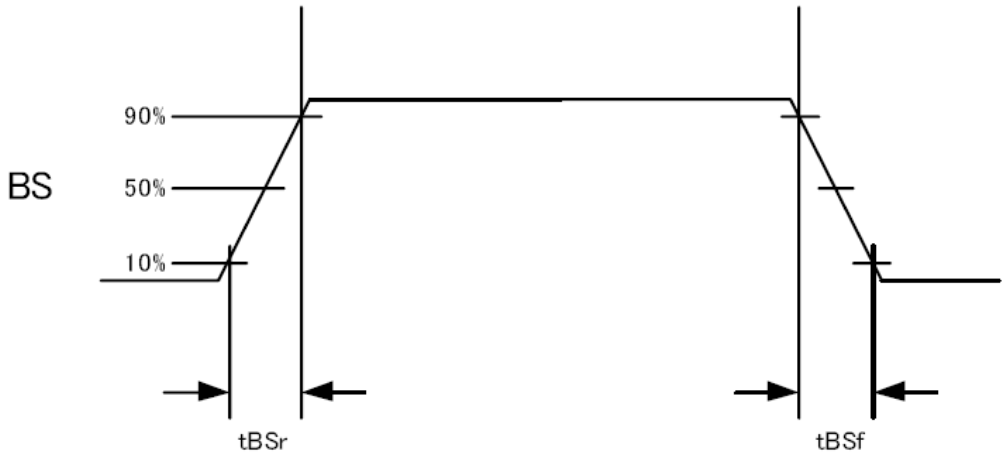
SD Spec. ver1.0 Timing

Parameter	Symbol	Min	Max	Unit	Remark
Clock Frequency Data transfer mode	fpp	0	25	MHz	CL<=100Pf
Clock Frequency identification mode	fOD	0~100	400	KHz	CL<=250pF
Clock Low Time	tWL	10		Ns	CL<=100pF
Clock High Time	TWH	10		Ns	CL<=100pF
Clock Rise Time	tTLH		10	Ns	CL<=100pF
Clock Fall Time	tTHL		10	Ns	CL<=100pF
Clock Low Time	tWL	50		Ns	CL<=100pF
Clock High Time	TWH	50		Ns	CL<=100pF
Clock Rise Time	tTLH		50	Ns	CL<=100pF
Clock Fall Time	tTHL		50	Ns	CL<=100pF
Input Set-up Time	tISU	5		Ns	CL<=25pF
Input Hold Time	tIH	5		Ns	CL<=25pF
Output Delay Time under Data Transfer Mode	tODLY		14	Ns	CL<=25pF
Output Delay time under identification transfer mode	tODLY		50	Ns	CL<=25pF

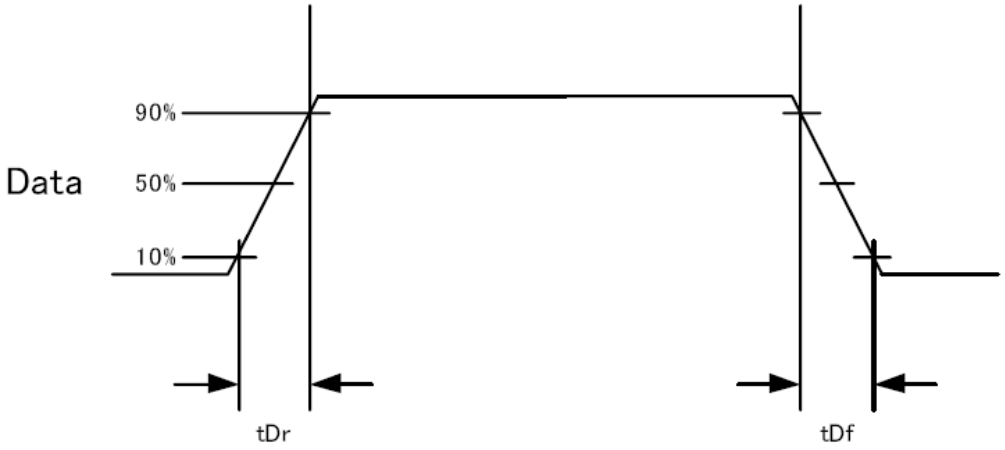
26.24 MS IF



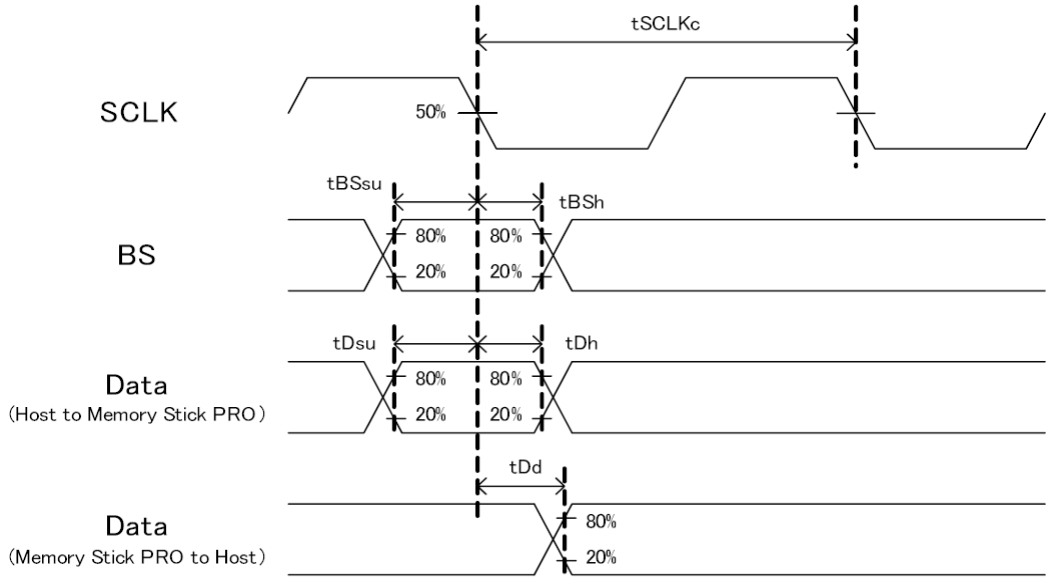
Serial Clock Timing



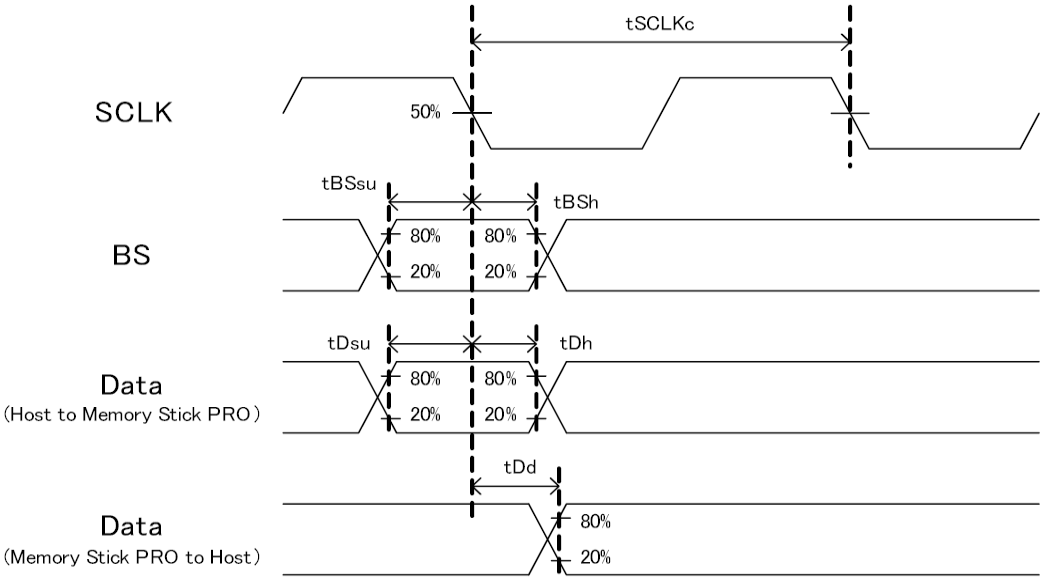
BS Timing



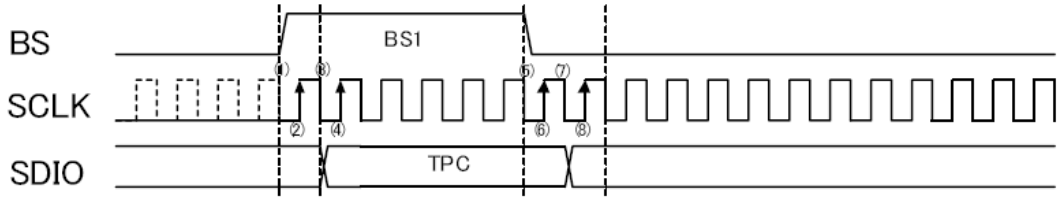
Data Timing



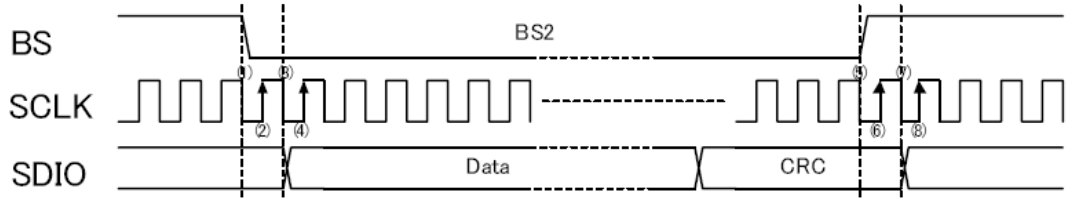
Transfer Operation Timing (Serial Interface)



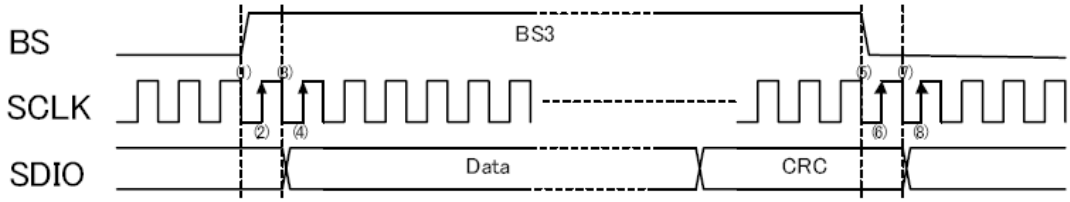
Transfer Operation Timing (Parallel Interface)



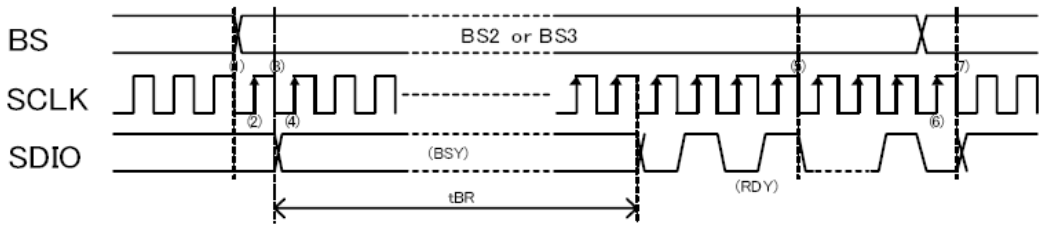
Serial Interface – TPC Transfer State (BS1)



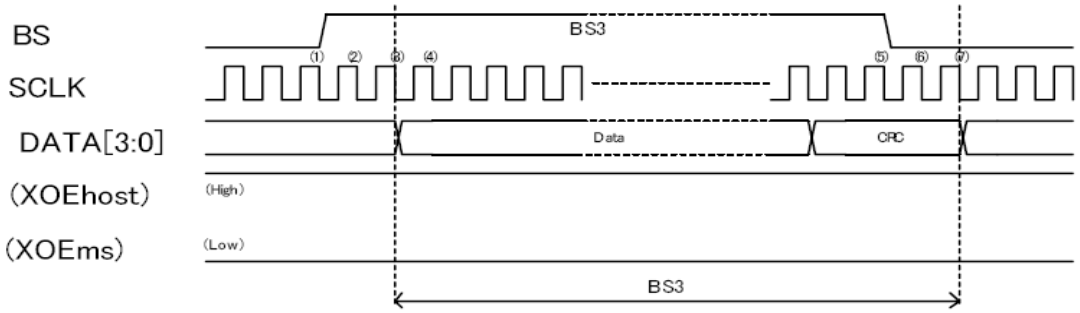
Serial Interface – TPC Transfer State (Write Packet: BS2)



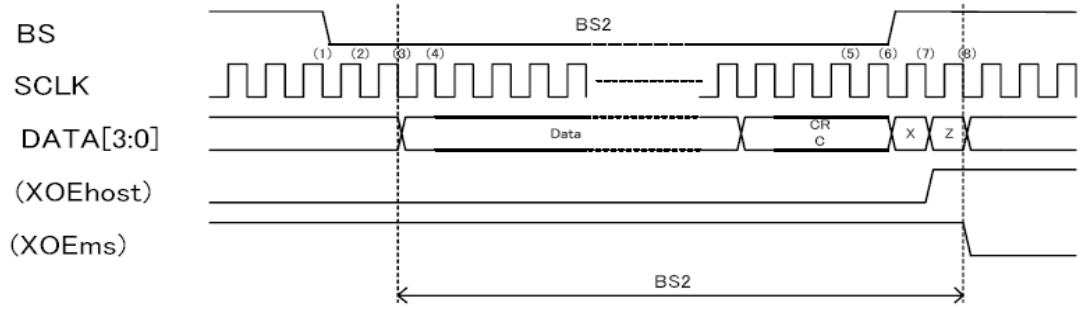
Serial Interface – TPC Transfer State (Read Packet: BS3)



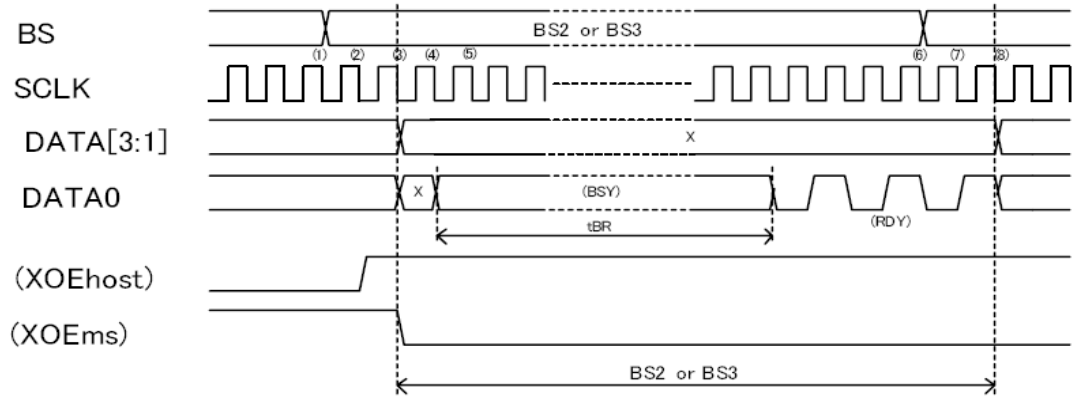
Serial Interface – Handshake State (Read Packet: BS2 / Write Packet: BS3)



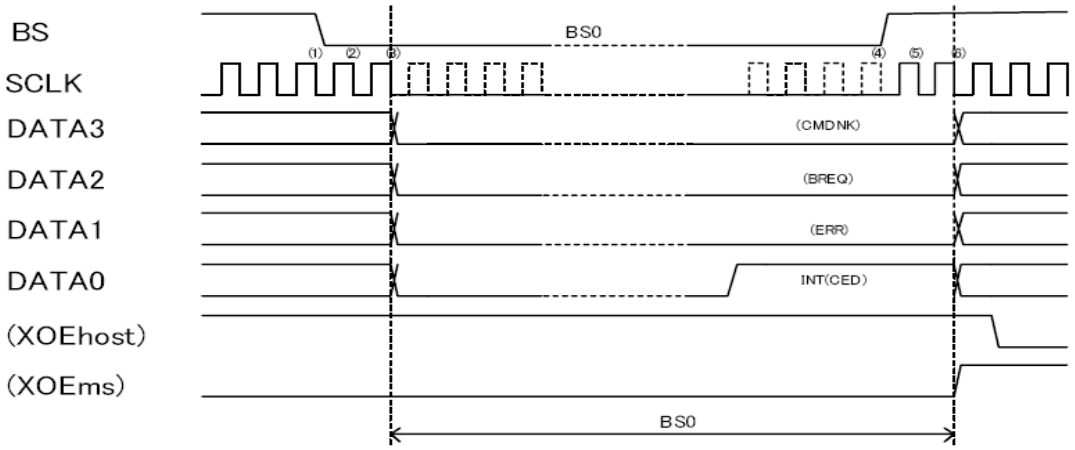
Parallel Interface – TPC Transfer State (Read Packet: BS3)



Parallel Interface – TPC Transfer State (Write Packet: BS2)



Parallel Interface –Handshake State (Read Packet: BS2 / Write Packet: BS3)



Parallel Interface – TPC transfer state (BS0)

Terminal function

Pin#	Terminal Name	I/O	Serial transfer	Parallel Transfer
1	Vss		Vss	
2	BS	O	Bus State Signal	
3	DATA1	I/O	Hi-Z	Data signal 1
4	DATA0/SDIO	I/O	Data signal	Data signal 0
5	DATA2	I/O	Hi-Z	Data signal 2
6	INS	I	Memory Stick Insertion detection	
7	DATA3	I/O	Hi-Z	Data signal 3
8	CLK	O	Clock signal	
9	VCC		Vcc	
10	VSS		Vss	

Characteristics of the Serial Interface

Measurement conditions: VCC=2.7~3.6[V], Ta=-5~65[℃]

Signal	Parameter	Symbol	Rating		Unit
			Min.	Max	
SCLK	Period	tSCLKc	50	-	nsec
	H pulse width	tSCLKwh	15	-	nsec
	L pulse width	tSCLKwl	15	-	nsec
	Rising time	tSCLKr	-	10	nsec
	Falling time	tSCLKf	-	10	nsec
	Setup time	tBSsu	5	-	nsec

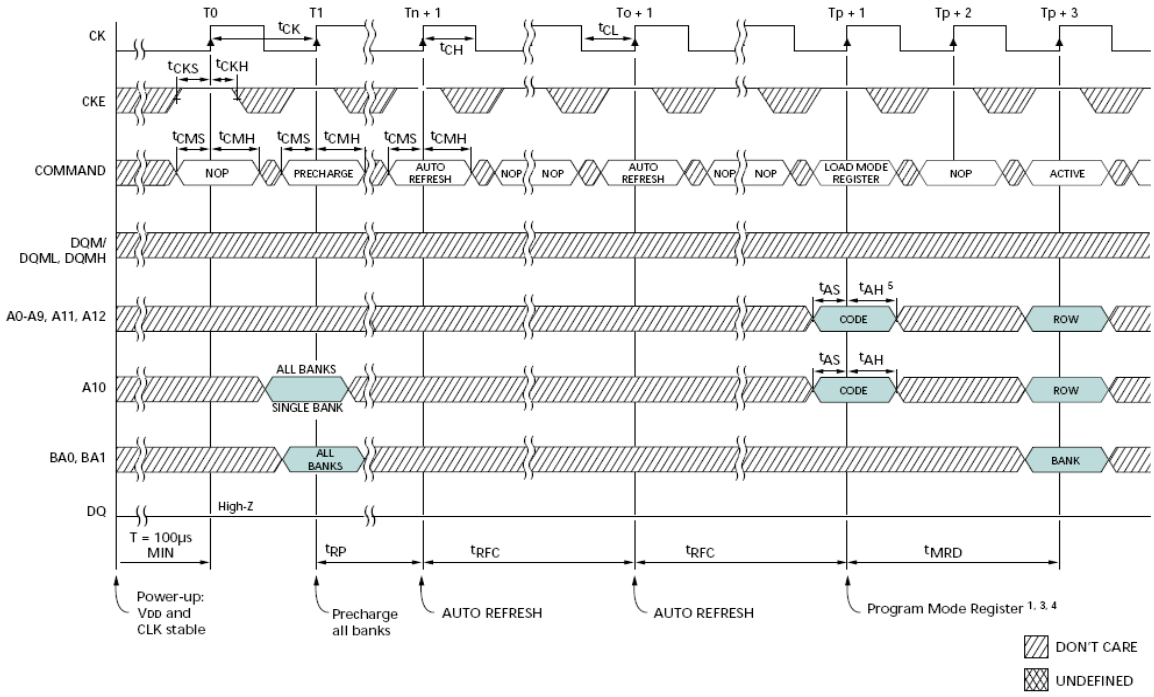
BS	Hold time	tBSh	5	-	nsec
	Rising time	tBSr	-	10	nsec
	Falling time	tBSf	-	10	nsec
DATA	Setup time	tDsu	5	-	nsec
	Hold time	tDh	5	-	nsec
	Rising time	tDr	-	10	nsec
	Falling time	tDf	-	10	nsec
	Output delay time	tDd	-	15	nsec

Characteristics of the Parallel Interface

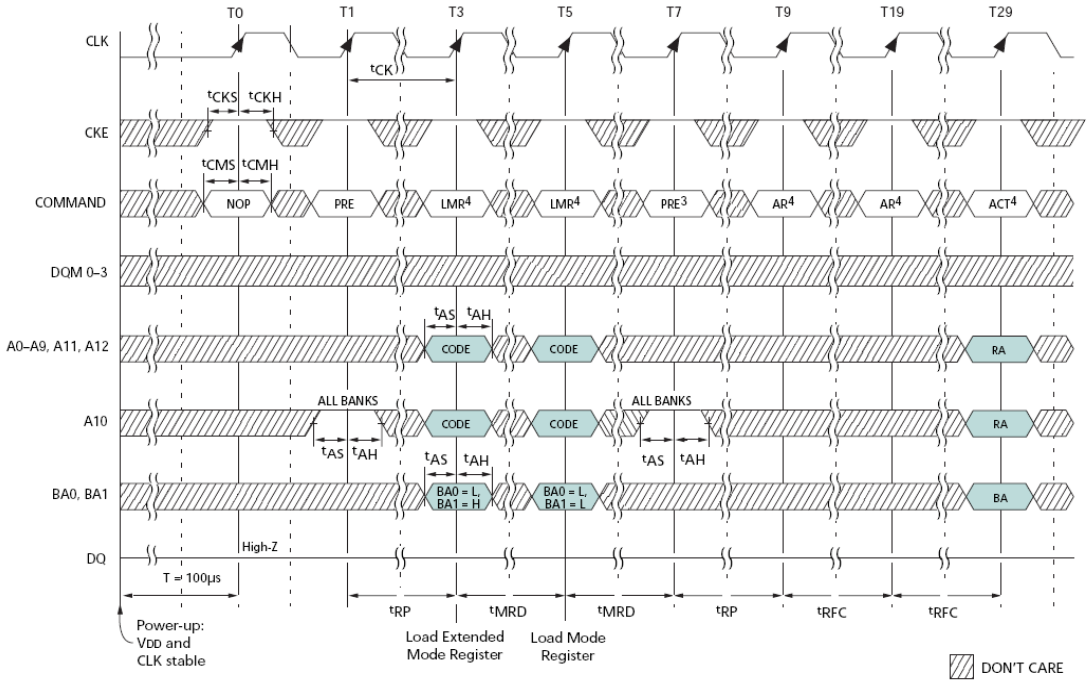
(Measurement conditions: VCC=2.7~3.6[V], Ta=-5~65[℃]

Signal	Parameter	Symbol	Rating		Unit
			Min.	Max	
SCLK	Period	tSCLKc	25	-	nsec
	H pulse width	tSCLKwh	5	-	nsec
	L pulse width	tSCLKwl	5	-	nsec
	Rising time	tSCLKr	-	10	nsec
	Falling time	tSCLKf	-	10	nsec
BS	Setup time	tBSsu	8	-	nsec
	Hold time	tBSh	1	-	nsec
	Rising time	tBSr	-	10	nsec
	Falling time	tBSf	-	10	nsec
DATA	Setup time	tDsu	8	-	nsec
	Hold time	tDh	1	-	nsec
	Rising time	tDr	-	10	nsec
	Falling time	tDf	-	10	nsec
	Output delay time	tDd	-	15	nsec

26.25 SDRAM IF



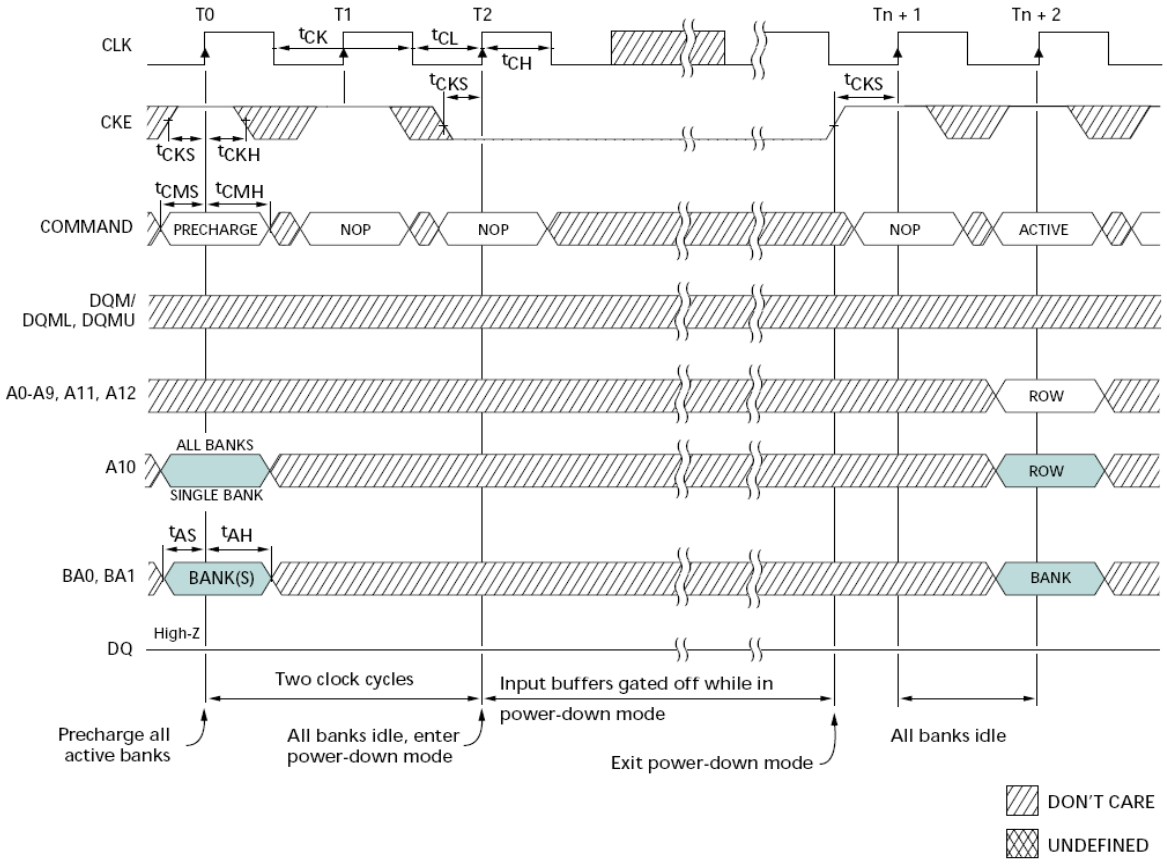
Standard SDRAM Power up Timing



Mobile SDRAM Power up Timing

NOTE:

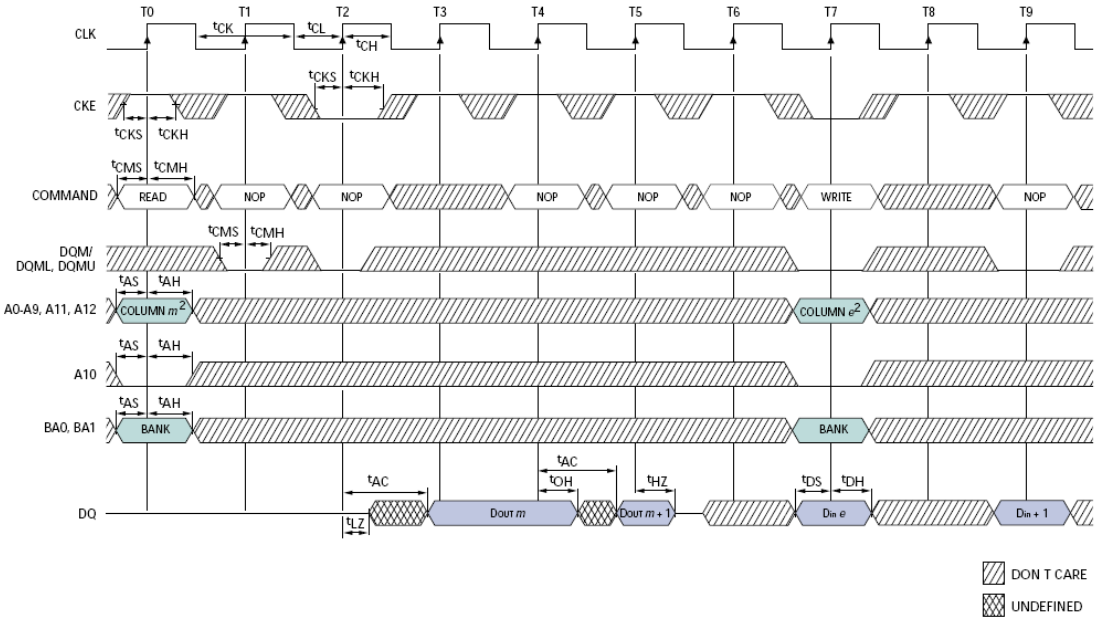
1. The Mode Register may be loaded prior to the AUTO REFRESH cycles if desired.
2. If CS is HIGH at clock high time, all commands applied are NOP.
3. Outputs are guaranteed High-Z after command is issued.
4. A12 should be LOW at t_P + 1.



SDRAM Power down Timing

NOTE:

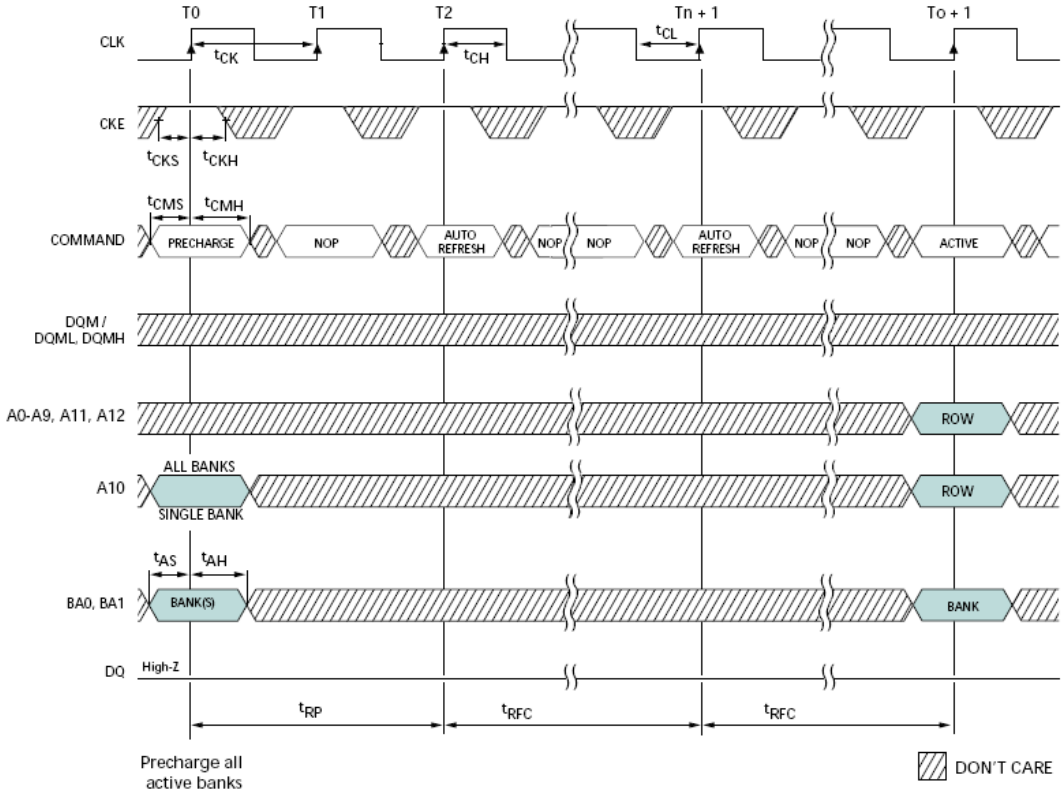
1. Violating refresh requirements during power-down may result in a loss of data.
2. CAS latency indicated in parentheses



SDRAM Clock Suspend

NOTE:

1. For this example, the burst length = 2, the CAS latency = 3, and AUTO PRECHARGE is disabled.
2. CAS latency indicated in parentheses

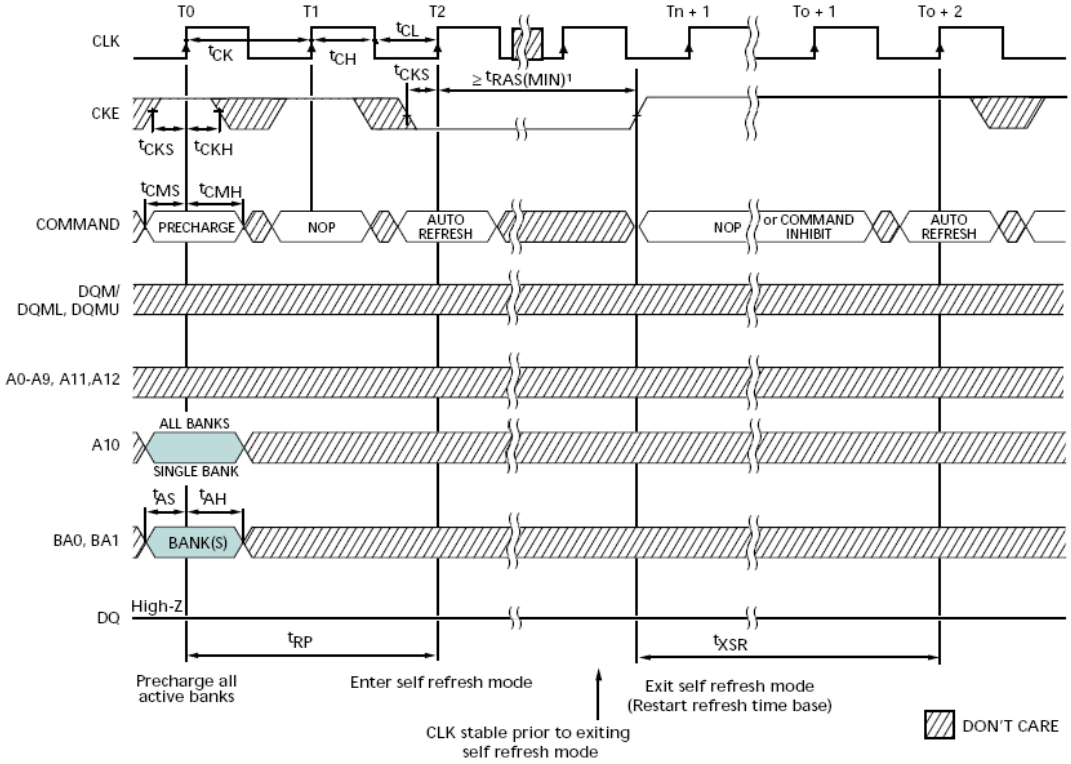


SDRAM Auto Refresh

NOTE:

1. CAS latency indicated in parentheses

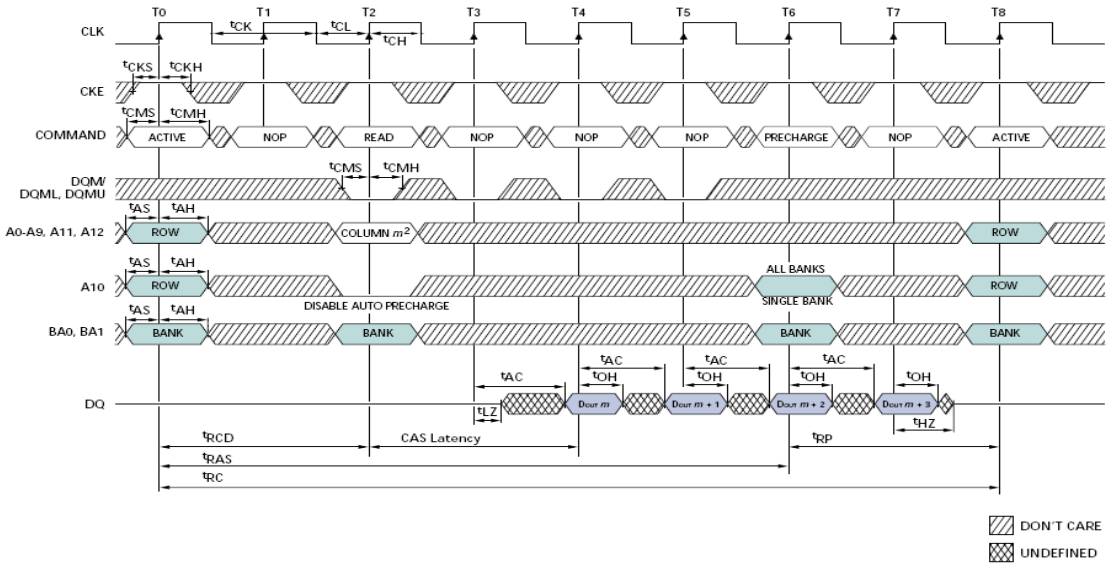
Self Refresh



SDRAM Self Refresh

NOTE:

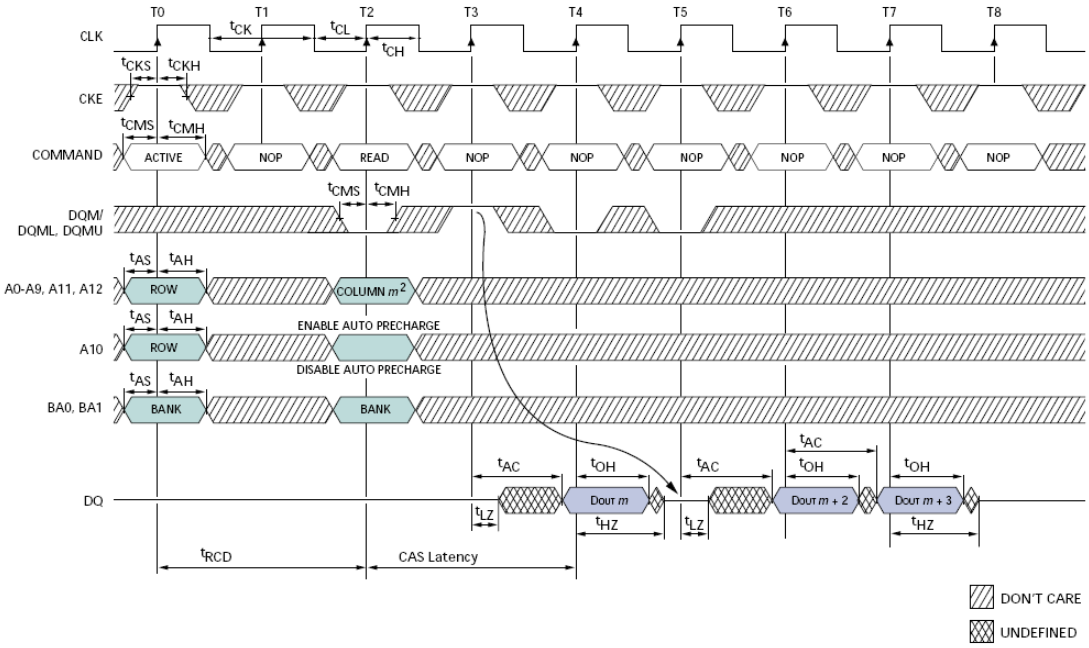
1. No maximum time limit for Self Refresh. $t_{RAS(MIN)}$ applies to non-Self Refresh mode.
2. t_{XSR} requires minimum of two clocks regardless of frequency or timing.
3. CAS latency indicated in parentheses



SDRAM Read

NOTE:

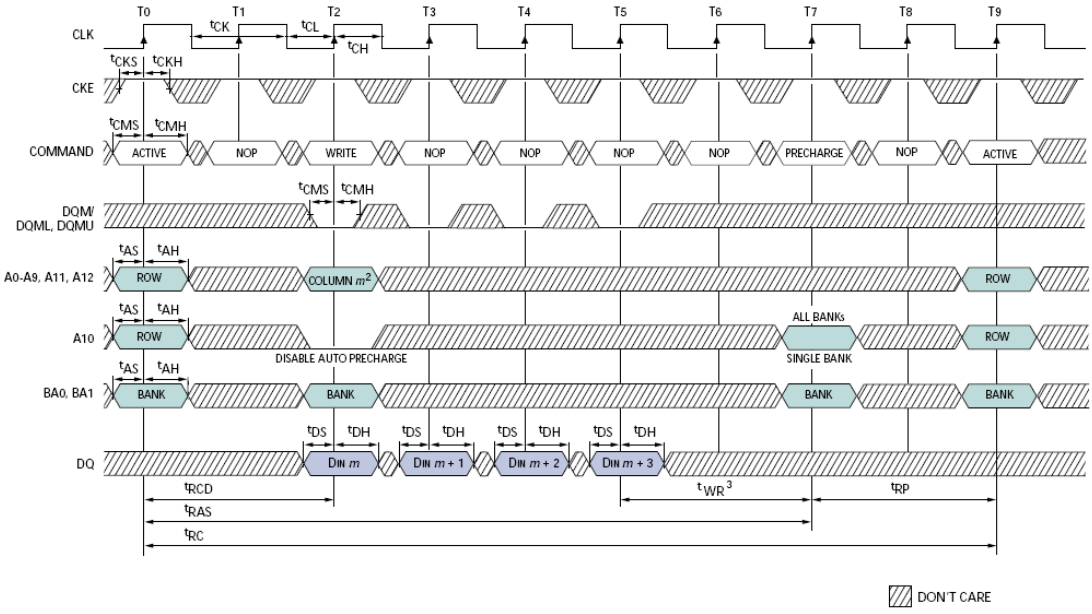
1. For this example, the burst length = 4, the CAS latency = 2, and the READ burst is followed by a “manual” PRECHARGE.
2. CAS latency indicated in parentheses



SDRAM Read DQM Operation

NOTE:

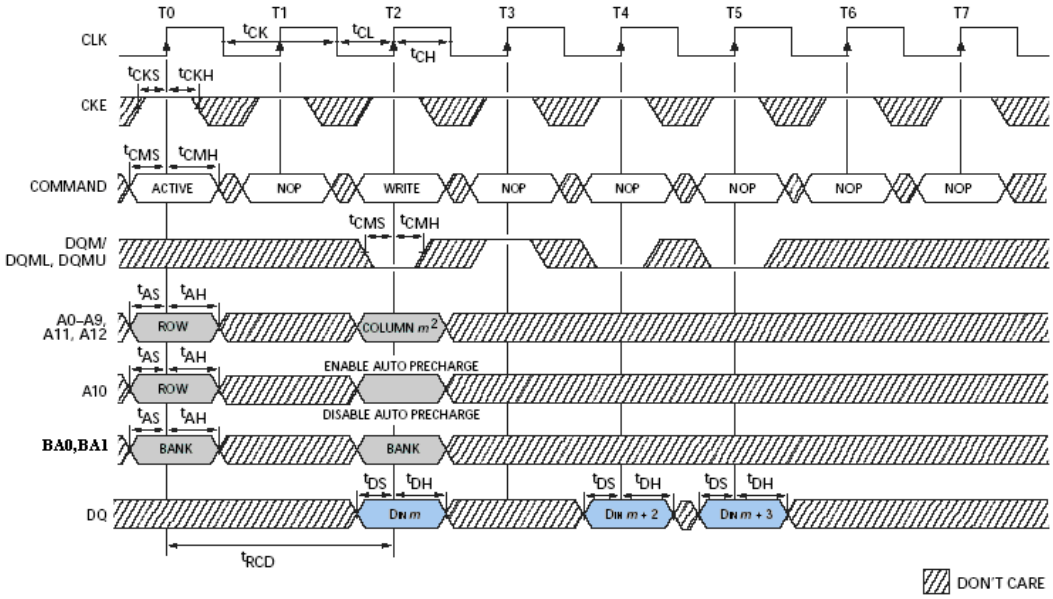
1. For this example, the burst length = 4, and the CAS latency = 2.
2. CAS latency indicated in parentheses.



SDRAM Write

NOTE:

1. For this example, the burst length = 4, and the WRITE burst is followed by a “manual” PRECHARGE.
2. 14ns to 15ns is required between <DIN m> and the PRECHARGE command, regardless of frequency.
3. CAS latency indicated in parentheses.



SDRAM Write-DQM Operation

NOTE:

1. For this example, the burst length = 4.
2. CAS latency indicated in parentheses.

SDRAM AC Characteristic

Ac Characteristics		Symbol	PC-100		
Parameter			Min	Max	Units
Access time from CLK (positive edge)	CL = 3	tAC (3)		7	ns
	CL = 2	tAC (2)		8	ns
Address hold time		tAH	1		ns
Address setup time		tAS	2.5		ns
CLK high-level width		tCH	3		ns
CLK low-level width		tCL	3		ns
Clock cycle time	CL = 3	tCK (3)	10		ns
	CL = 2	tCK (2)	12		ns
CKE hold time		tCKH	1		ns
CKE setup time		tCKS	2.5		ns
CS#, RAS#, CAS#, WE#, DQM hold time		tCMH	1		ns
CS#, RAS#, CAS#, WE#, DQM setup time		tCMS	2.5		ns
Data-in hold time		tDH	1		ns
Data-in setup time		tDS	2.5		ns
Data-out High-Z time	CL = 3	tHZ (3)		7	ns
	CL = 2	tHZ (2)		8	ns
Data-out Low-Z time		tLZ	1		ns
Data-out hold time (load)		tOH	2.5		ns
Data-out hold time (no load)		tOHN	1.8		ns
ACTIVE-to-PRECHARGE command		tRAS	50	120,000	ns
ACTIVE-to-ACTIVE command period		tRC	100		ns
ACTIVE-to-READ or WRITE delay		tRCD	20		ns
Refresh period		tREF		64	ms
AUTO REFRESH command period		tRFC	100		ns
PRECHARGE command period		tRP	20		ns

ACTIVE bank a to ACTIVE bank b command	tRRD	2		tCK
Transition time	tT	0.5	1.2	ns
WRITE recovery time Auto precharge mode (a)	tWR (a)	1 CLK +5ns		–
Manual precharge mode (m)	tWR (m)	15		ns
Exit SELF REFRESH to ACTIVE command	tXSR	100		ns

27 Pin Definition

27.1 Pin Sort by Pin Number

ATJ 2259B	Pin Name	Pin Function	I/O Type	Driver	Short Description
1	RTCVDD	RTCVDD	PWRI	/	RTC Power VDD
2	LOSCI	LOSCI	AI	/	Low Oscillator Input
3	LOSCO	LOSCO	AO	/	Low Oscillator Output
4	NF_CEB3	NOR_CEB5	O	4mA	Nor Flash CE5
		LDC_CE			LDC Interface CE
		NF_CEB3			NAND Flash Interface CE3
		GPIOB28	BI		GPIOB Port 28
5	NF_CEB0	NOR_CEB4	O	4mA	NOR Flash CE4
		LDC_CE			LDC Interface CE
		NF_CEB0			NAND Flash Interface CE0
		GPIOB27	BI		GPIOB Port 27
6	NF_CEB2	NF_CEB2	O	4mA	NAND Flash Interface CE2
		NOR_CEB2			Nor Flash Interface CE2
		LDC_CE			LDC Interface CE
		SD_CLK1			SD CARD Interface CLOCK1
		GPIOA17	BI		GPIOA Port 17
7	NF_CEB1	NF_CEB1	O	4mA	NAND flash Interface CE1
		NOR_CEB1			Nor flash Interface CE1
		LDC_CE			LDC Interface CE
8	BTD6	BT656_D[6]	BI	4mA	BT656 Interface Data 6
		NOR_A[12]			Nor flash Interface Address 12
		LDR_D7			LDR interface Data 7
		GPIOB6	BI		GPIOB port 6
9	SIRQ1	SIRQ1	I	2mA	External IRQ 1
		GPIOB31	BI		GPIOB port 31
10	LDRD3	NOR_A[3]	BI	4mA	Nor Flash Interface Address 3
		LDR_D3			LDR interface Data 3

		GPIOA3	BI		GPIOA Port 3
11	LDRD4	NOR_A[4]	I	4mA	Nor flash Interface Address 4
		LDC_WRB			LDC Interface WR
		NOR_WRB			Nor flash Interface WR
		LDR_D4			LDR interface Data 4
		GPIOA4	BI		GPIOA Port 4
12	DRVVBUS	DRVVBUS	O	2mA	USB Interface VBUS
		NOR_RDB			Nor flash Interface RD
		LDC_RDB			LDC Interface RD
		GPIOA15	BI		GPIOA Port 15
13	GPIOB26	NF_RB	I	2mA	NAND flash Interface Read/Busy
		GPIOB26	BI		GPIOB Port 26
14	WRB	NF_WR	O	8mA	NAND flash Interface WR
		NOR_WRB			Nor flash Interface WR
		LDC_WRB			LDC Interface WR
15	BTD7	BT656_D[7]	BI	4mA	BT656 Interface Data 7
		NOR_A[13]			Nor flash Address13
		LDR_DE			LDR interface DE
		GPIOB7	BI		GPIOB Port 7
16	RDB	NF_RD	O	16mA	NAND Flash Interface RD
		NOR_RDB			Nor Flash Interface RD
		LDC_RDB			LDC Interface RD
17	LDRD5	NOR_A[5]	O	4mA	Nor flash Interface Address 5
		LDC_RDB			LDC Interface RD
		NOR_RDB			Nor flash Interface RD
		LDR_D5			LDR interface Data 5
		GPIOA5	BI		GPIOA Port 5
18	BTPCLK	BT656_PCLK	BI	4mA	BT656 Interface PCLK
		NOR_A[14]			Nor flash Address 14
		LDR_DCLK			LDR interface clock
		GPIOB8	BI		GPIOB Port 8
19	BTMCLK	BT656_CLKOUT	BI	8mA	BT656 Interface CLKOUT
		NOR_A[17]			Nor Flash Interface Address 17
		LDR_D2			LDR Interface Data 2

		GPIOB11	BI		GPIOB Port 11
20	KSIN6	KS_IN[6]	BI	2mA	Key scan Input 6
		GPIOB20	BI		GPIOB port 20
21	VDD	MVDD	PWRI	/	VDD
22	VCC	VCC	PWRI	/	VCC
23	GND	GND	PWR	/	GND
24	SDRBA0	SDRAM_BA0	O	8mA	SDRAM Interface bank address0
25	SDRDQ0	SDRAM_DQ0	BI	8mA	SDRAM Interface data 0
26	SDRA0	SDRAM_A0	O	8mA	SDRAM Interface address 0
27	SDRA1	SDRAM_A1	O	8mA	SDRAM Interface Address 1
28	SDRDQ1	SDRAM_DQ1	BI	8mA	SDRAM Interface Data 1
29	SDRA2	SDRAM_A2	O	8mA	SDRAM Interface Address2
30	SDRBA1	SDRAM_BA1	O	8mA	SDRAM Interface Bank Address 1
31	SDRA3	SDRAM_A3	O	8mA	SDRAM Interface Address3
32	SDRDQ2	SDRAM_DQ2	BI	8mA	SDRAM Interface Data2
33	SDRA4	SDRAM_A4	O	8mA	SDRAM Interface Address4
34	SDRA5	SDRAM_A5	O	8mA	SDRAM Interface Address 5
35	SDRDQ3	SDRAM_DQ3	BI	8mA	SDRAM Interface Data3
36	SDRA6	SDRAM_A6	O	8mA	SDRAM Interface Address 6
37	SDRVP	SDRAM_VP	PWRI	/	SDRAM Interface Power
38	GND	GND	PWR	/	GND
39	SDRDQ4	SDRAM_DQ4	BI	8mA	SDRAM Interface Data 4
40	SDRA7	SDRAM_A7	O	8mA	SDRAM Interface Address 7
41	SDRA8	SDRAM_A8	O	8mA	SDRAM Interface Address 8
42	SDRDQ5	SDRAM_DQ5	BI	8mA	SDRAM Interface Data 5
43	SDRA9	SDRAM_A9	O	8mA	SDRAM Interface Address 9
44	SDRA10	SDRAM_A10	O	8mA	SDRAM Address 10
45	SDRDQ6	SDRAM_DQ6	BI	8mA	SDRAM Interface Data 6
46	SDRA11	SDRAM_A11	O	8mA	SDRAM Interface Address11
		GPIOA25	BI		GPIOA port 25
47	SDRDQ7	SDRAM_DQ7	BI	8mA	SDRAM Interface Data7
48	SDRWEB	SDRAM_WEB	O	8mA	SDRAM Interface Write Enable
49	SDRDQ8	SDRAM_DQ8	BI	8mA	SDRAM Interface Data 8
50	SDRA12	SDRAM_A12	O	8mA	SDRAM Interface Address12
		GPIOA26	BI		GPIOA Port 26

51	SDRDQ9	SDRAM_DQ9	BI	8mA	SDRAM Interface Data 9
52	SDRDQ10	SDRAM_DQ10	BI	8mA	SDRAM Interface Data10
53	SDRDQ11	SDRAM_DQ11	BI	8mA	SDRAM Interface Data11
54	SDRDQ12	SDRAM_DQ12	BI	8mA	SDRAM interface Data 12
55	SDRRASB	SDRAM_RASB	O	8mA	SDRAM interface RAS
56	SDRCASB	SDRAM_CASB	O	8mA	SDRAM Interface CAS
57	SDRDQ13	SDRAM_DQ13	BI	8mA	SDRAM Interface Data13
58	SDRCSB	SDRAM_CSB	O	8mA	SDRAM Interface CS
59	GND	GND	PWR	/	GND
60	SDRVP	SDRAM_VP	PWRI	/	SDRAM Interface Power
61	SDRCK	SDRAM_CK	O	16mA	SDRAM Interface Clock
62	SDRCKE	SDRAM_CKE	O	16mA	SDRAM Interface Clock Enable
63	SDRDQM0	SDRAM_LDQM	O	8mA	SDRAM interface LDQM(for 16bits SDRAM)
		SDRAM_DQM[0]			SDRAM Interface DQM0
64	SDRDQ14	SDRAM_DQ14	BI	8mA	SDRAM Data14
65	SDRDQM1	SDRAM_DQM	O	8mA	SDRAM Interface DQM(for 8bits SDRAM)
		UDQM			SDRAM Interface UDQM(for 16bits SDRAM)
		SDRAM_DQM[1]			SDRAM Interface DQM1
66	SDRDQ15	SDRAM_DQ15	BI	8mA	SDRAM Interface Data15
67	VCC	VCC	PWRI	/	VCC
68	LDRHSYNC	SDRAM_DQ28	BI	8mA	SDRAM Interface Data 28
		LDR_HSYNC			LDR interface HSYNC
		GPIOA21	BI		GPIOA Port 21
69	LDRVSYNC	SDRAM_DQ2	BI	8mA	SDRAM Interface Data 27

		7			
		LDR_VSYNC			LDR Interface VSYNC
		GPIOA20	BI		GPIOA port 20
70	LDRD12	SDRAM_DQ19	BI	8mA	SDRAM Interface Data19
		LDR_D12			LDR Interface Data 12
		GPIOA18	BI		GPIOA port 18
71	LDRD13	SDRAM_DQ29	BI	8mA	SDRAM Interface data 29
		LDR_D13			LDR Interface Data 13
		GPIOA22	BI		GPIOA Port A 22
72	LDRD10	SDRAM_DQ30	BI	8mA	SDRAM Interface Data 30
		LDR_D10			LDR Interface Data 10
		GPIOA23	BI		GPIOA Port 23
73	LDRD11	SDRAM_DQ31	BI	8mA	SDRAM Interface Data 31
		LDR_D11			LDR Interface Data 11
		GPIOA24	BI		GPIOA Port 24
74	LDRD21	SDRAM_DQ26	BI	8mA	SDRAM Interface Data 26
		LDR_D21			LDR interface Data 21
		GPIOA19	BI		GPIOA Port 19
75	VDD	VDD	PWRI	/	VDD
76	VBUS	VBUS	AI	/	USB Interface VBUS
77	ID	ID	I	/	USB Interface ID
78	UVCC	UVCC	PWRI	/	USB Interface UVCC
79	DP	HSDP	BI	/	USB Interface Data Plus
80	DM	HSDM	BI	/	USB Interface Data Minus
81	UGND	UGND	PWR		USB interface GND
82	RREF	RREF	AO	/	USB Interface Reference Resistance
83	UGND	UGND	PWR	/	USB Interface UGND
84	UART1RX	UART1_RX	BI	2mA	Uart1 Interface RX
		SPI_MISO			SPI Interface MISO
		I2C2_SDA			I2C2 Interface SDA
		SPDIF_RX			SPDIF Interface RX
		LDR_PWM0			LDR Interface PWM0

		GPIOB15	BI		GPIOB Port 15
85	UART1TX	UART1_TX	BI	2mA	Uart1 Interface Tx
		SPI_SS			SPI Interface Slave Selection
		I2C2_SCL			I2C2 interface SCL
		SPDIF_TX			SPDIF interface TX
		LDR_PWM1			LDR Interface PWM1
		GPIOB14	BI		GPIOB Port 14
86	MICINR	MICINR	AI	/	Microphone in Right channel
	MICINL	MICINL	AI	/	Microphone In Left Channel
87	VMIC	VMIC	AI	/	Microphone Power Supply
88	*FMINR*	FMINR	AI	/	FM In Right Channel
89	*FMINL*	FMINL	AI	/	FM in Left Channel
90	*LINEINR*	LINEINR	AI	/	Line in Right Channel
91	*LINEINL*	LINEINL	AI	/	Line in Left Channel
92	AGND	AGND	PWR	/	Audio Analog GND
93	AVCC	AVCC	PWRO	/	Audio Analog VCC
94	VRDA	VRDA	AO	/	Audio DAC Voltage Reference
95	VREFI	VREFI	AI	/	Voltage Reference Input
96	PAGND	PAGND	PWR	/	Audio PA GND
97	AOUTR	AOUTR	AO	/	Audio output Right Channel
98	PAVCC	PAVCC	PWRO	/	Audio PA VCC
99	AOUTL	AOUTL	AO	/	Audio output Left Channel
100	*TVCVBS*	TVCVBS	AO	/	Video CVBS signal Output
101	*TVRREF*	TVRREF	AO	/	TV reference Resistance
102	Y2	Y2	ABI	/	Touch Panel analog input Y2
103	Y1	Y1	ABI	/	Touch Panel analog input Y1
104	X2	X2	ABI	/	Touch Panel analog input X2
105	X1	X1	ABI	/	Touch Panel analog input X1
106	AVDD	AVDD	PWRO	/	Audio VDD
107	HOSCO	HOSCO	AI	/	High Oscillator Input
108	HOSCI	HOSCI	AO	/	High Oscillator Output
109	VCC	VCC	PWRI	/	VCC
110	VDD	VDD	PWRI	/	VDD
111	KSIN2	KS_IN[2]	BI	2mA	Key Scan Input2
		GPIOA10	BI		GPIOA Port 10
112	KSOUT2	KS_OUT[2]	BI	2mA	Key Scan output 2
		GPIOB22	BI		GPIOB Port 22
113	KSIN1	KS_IN[1]	BI	2mA	Key Scan Input 1

		GPIOA9	BI		GPIOA Port 9
114	KSOUT1	KS_OUT[1]	BI	2mA	Key Scan Output 1
		GPIOA13	BI		GPIOA Port 13
115	KSIN0	KS_IN[0]	BI	2mA	KEY Scan in 0
		GPIOA8	BI		GPIOA Port 8
116	KSOUT0	KS_OUT[0]	BI	2mA	Key Scan Output 0
		GPIOA12	BI		GPIOA Port12
117	LDRDE	NOR_CEB3	O	4mA	NOR flash Interface CE3
		NF_CEB3			NAND flash interface CE3
		LDR_DE			LDR Interface DE
118	RESET	RESETB	I	/	System RESET
119	TEST	TEST	I	/	TEST
		CLKOUT	O		FM Module Clock out
		BT656_CLKOUT			BT656 Interface Clock
120	BTD5	BT656_D[5]	BI	4mA	BT656 Interface Data 5
		NOR_A[11]			Nor Flash A 11
		LDR_D6			LDR Interface Data 6
		GPIOB5	BI		GPIOB Port 5
121	BTD4	BT656_D[4]	BI	4mA	BT656 Interface Data 4
		NOR_A[10]			Nor flash Interface Address 10
		LDR_D5			LDR Interface Data 5
		GPIOB4	BI		GPIOB port 4
122	GPIOB16	SPDIF_TX	BI	2mA	SPDIF Interface TX
		I2C1_SCL			I2C1 interface SCL
		UART2IR_TX			UART2 or IrDA Interface TX
		LDR_D18			LDR Interface Data 18
		GPIOB16	BI		GPIOB Port 16
123	LDRD22	SPDIF_RX	BI	2mA	SPDIF interface RX
		I2C1_SDA			I2C Interface SDA
		UART2IR_RX			UART2 or IrDA interface RX
		LDR_D22			LDR Interface Data 22
		GPIOB17	BI		GPIOB Port 17
124	I2C1SDA	I2C1_SDA	BI	2mA	I2C1 Interface SDA
		UART2IR_RX			Uart2 or IrDA interface Rx
		UART1_CTSB			Uart1 Interface CTS
		SPI_MOSI			SPI Interface Master Output

					Slave in
		GPIOA7	BI		GPIOA Port 7
125	I2C1SCL	I2C1_SCL	BI	2mA	I2C1 Interface SCL
		UART2IR_TX			Uart2 or IrDA Interface Tx
		UART1_RTSB			Uart1 Interface RTS
		SPI_SCK			SPI Interface Clock
		GPIOA6	BI		GPIOA Port 6
126	BTVSYNC	BT656_VSYNC	BI	2mA	BT656 Interface VSYNC
		NOR_A[16]			NOR flash address16
		LDR_VSYNC			LDR Interface VSYNC
		GPIOB10	BI		GPIOB Port 10
127	BTHSYNC	BT656_HSYNC	BI	2mA	BT656 Interface HSYNC
		NOR_A[15]			Nor flash Address 15
		LDR_HSYNC			LDR Interface HSYNC
		GPIOB9	BI		GPIOB port 9
128	BL_NDR	BL_NDR	AO	/	Back Light NDR
129	REM_CON	REM_CON	AI	/	Remote Control ADC input
130	IO_VDD	IO_VDD	PWR	/	POW Pin IOVDD
131	LXVDD	LXVDD	PWR	/	POW Pin LXVDD
132	PGND	PGND	PWR	/	POWER MOS GND
133	IO_VCC	IO_VCC	PWR	/	POW Pin IOVCC
134	BAT	BAT	PWRI	/	Battery input
135	DC5V	DC5V	PWRI	/	DC5V input
136	VCC	VCC	PWRIO	/	VCC
137	VDD	VDD	PWRIO	/	VDD
138	VCCOUT	VCCOUT	PWRO	/	Programmed VCC output
139	GND	GND	PWR	/	GND
140	SIRQ0	SIRQ0	I	2mA	External IRQ 0
		GPIOA31	BI		GPIOA Port 31
141	SD_CLK	SD_CLK0	O	16mA	SD CARD Interface CLOCK0
		CE6			Nor Flash Interface CE6
		MS_CLK			MS Card Interface CLOCK
		GPIOB29	BI		GPIOB Port 29
142	LDRD14	I2S_BCLK	BI	2mA	I2S Interface Bit Clock
		PCM_CLK			PCM Interface Clock

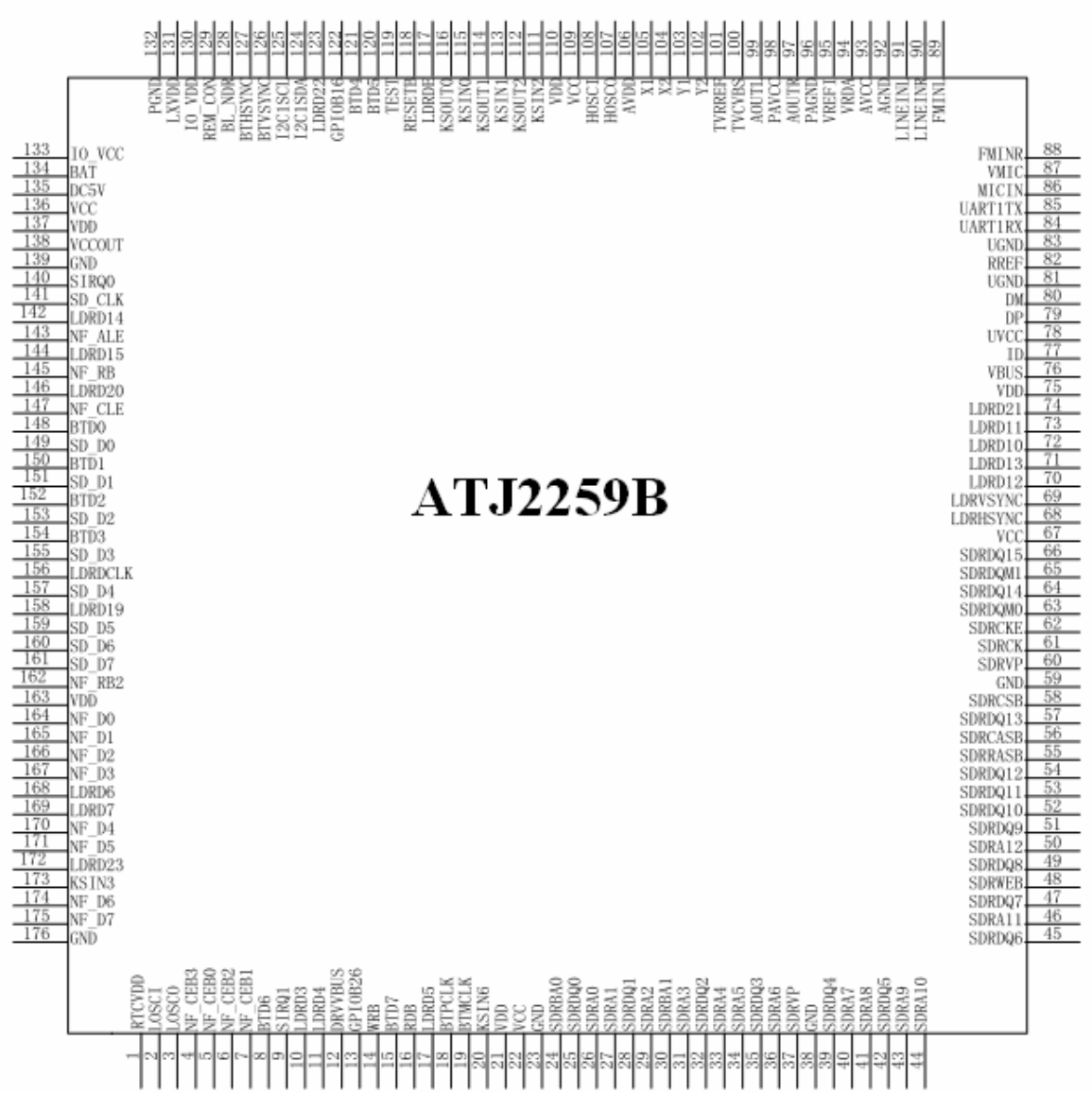
		NOR_A[19]			Nor flash Interface Address 19
		LDR_D14			LDR Interface Data 14
		GPIOA28	BI		GPIO A port 28
143	NF_ALE	NF_ALE	O	4mA	NAND flash ALE
		NOR_A[0]			Nor flash Interface Address 0
		LDC_WD[0]			LDC Interface Data0
		GPIOA0	BI		GPIOA Port 0
144	LDRD15	I2S_LRCLK	BI	2mA	I2S Interface Left/Right Clock
		PCM_SYNC			PCM Sync Clock
		NOR_A[20]			Nor flash Interface Address 20
		LDR_D15			LDR Interface Data 15
		GPIOA29	BI		GPIOA Port 29
145	NF_RB	NF_RB	O	4mA	NAND flash interface Ready/Busy
		NOR_A[1]			Nor flash Interface Address 1
		LDC_WD[9]			LDC Interface data 9
		GPIOA1	BI		GPIOA Port 1
146	LDRD20	I2S_MCLK	BI	4mA	I2S Interface MCLK
		NOR_A[22]			Nor Flash Interface Address 22
		LDR_D20			LDR Interface Data 20
		GPIOB30	BI		GPIOB Port 30
147	NF_CLE	NF_CLE	O	4mA	NAND flash interface CLE
		NOR_A[2]			Nor flash interface address 2
		LDC_RS			LDC Interface RS
		SD_CMD			SD card Interface CMD
		MS_BS			MS Card Interface Bus State Signal
		GPIOA2	BI		GPIOA Port 2
148	BTD0	BT656_D[0]	BI	4mA	BT656 Interface Data 0
		NOR_A[6]			Nor flash Address 6
		LDR_D0			LDR Interface Data 0
		GPIOB0	BI		GPIOB Port 0
149	SD_D0	NF_D[8]	BI	4mA	NAND flash Data 8
		NOR_D[0]			Nor Flash Data 0

		LDC_WD[1]			LDC Interface data 1
		SD_DAT[0]			SD Card interface Data 0
		MS_D[0]			MS Card Interface Data 0
150	BTD1	BT656_D[1]	BI	4mA	Bt656 Interface Data 1
		NOR_A[7]			Nor flash Interface Address 7
		LDR_D1			LDR Interface Data 1
		GPIOB1	BI		GPIOB Port 1
151	SD_D1	NF_D[9]	BI	4mA	NAND Flash interface Data 9
		NOR_D[1]			Nor flash Interface Data 1
		LDC_WD[2]			LDC Interface data 2
		SD_DAT[1]			SD Card Interface Data 1
		MS_D[1]			MS Card Interface Data 1
152	BTD2	BT656_D[2]	BI	4mA	BT656 Interface Data 2
		NOR_A[8]			Nor Flash Interface Address 8
		LDR_D3			LDR Interface Data 3
		GPIOB2	BI		GPIOB Port 2
153	SD_D2	NF_D[10]	BI	4mA	NAND Flash interface Data 10
		NOR_D[2]			Nor flash Interface Data 2
		LDC_WD[3]			LDC Interface Data 3
		SD_DAT[2]			SD Card Interface Data 2
		MS_D[2]			MS Card Interface Data 2
154	BTD3	BT656_D[3]	BI	4mA	BT656 Interface Data 3
		NOR_A[9]			Nor Flash interface Address 9
		LDR_D4			LDR Interface Data 4
		GPIOB3	BI		GPIOB Port 3
155	SD_D3	NF_D[11]	BI	4mA	NAND flash Interface Data 11
		NOR_D[3]			Nor Flash Interface Data 3
		LDC_WD[4]			LDC Interface Data 4
		SD_DAT[3]			SD Card Interface Data 3
		MS_D[3]			MS Card Interface Data 3
156	LDRDCLK	I2S_OUT	BI	2mA	I2S Interface Data Out
		PCM_OUT			PCM Interface Data Out
		NOR_A[18]			Nor flash Interface Address 18
		SPDIF_TX			SPDIF Interface TX

		LDR_DCLK			LDR Interface clock
		GPIOA27	BI		GPIOA Port 27
157	SD_D4	NF_D[12]	BI	4mA	NAND flash Interface Data 12
		NOR_D[4]			Nor flash Interface Data 4
		LDC_WD[5]			LDC Interface data 5
		SD_DAT[4]			SD Card Interface Data 4
158	LDRD19	I2S_IN	BI	4mA	I2S Interface Data In
		I2S_MCLK			I2S Interface MCLK
		PCM_IN			PCM Interface Data In
		NOR_A[21]			NOR flash Interface Address 21
		SPDIF_RX			SPDIF Interface RX
		LDR_D19			LDR Interface Data 19
		GPIOA30	BI		GPIOA Port 30
159	SD_D5	NF_D[13]	BI	4mA	NAND flash Interface Data 13
		NOR_D[5]			Nor flash Interface Data 5
		LDC_WD[6]			LDC Interface data 6
		SD_DAT[5]			SD card Interface Data 5
160	SD_D6	NF_D[14]	BI	4mA	NAND flash Interface Data 14
		NOR_D[6]			Nor flash interface Data 6
		LDC_WD[7]			LDC Interface Data 7
		SD_DAT[6]			SD card interface Data 6
161	SD_D7	NF_D[15]	BI	4mA	NAND flash interface Data 15
		NOR_D[7]			Nor flash Interface Data 7
		LDC_WD[8]			LDC Interface Data 8
		SD_DAT[7]			SD card Interface data 7
162	NF_RB2	NOR_CEB0	O	4mA	Nor flash Interface CE0
		NF_CEB0			NAND flash interface CE0
		RB2			NAND flash Interface Read/Busy 2
		GPIOA16	BI		GPIOA Port 16
163	VDD	VDD	PWRI	/	VDD
164	NF_D0	NF_D[0]	BI	4mA	NAND flash Data 0
		NOR_D[8]			Nor flash Data 8

		LDC_WD[10]			LDC Interface Data 10
165	NF_D2	NF_D[1]	BI	4mA	NAND flash interface Data 1
		NOR_D[9]			Nor flash interface Data 9
		LDC_WD[11]			LDC Interface Data 11
166	NF_D2	NF_D[2]	BI	4mA	NAND flash interface Data 2
		NOR_D[10]			Nor flash interface Data 10
		LDC_WD[12]			LDC Interface data 12
167	NF_D3	NF_D[3]	BI	4mA	NAND flash interface 3
		NOR_D[11]			Nor flash Data 11
		LDC_WD[13]			LDC Interface Data 13
168	LDRD6	SDRAM_DQM[2]	O	8mA	SDRAM Interface DQM2
		LDR_D6			LDR Interface Data 6
169	LDRD7	SDRAM_DQM[3]	O	8mA	SDRAM Interface DQM3
		LDR_D7			LDR Interface Data 7
170	NF_D4	NF_D[4]	BI	4mA	NAND flash data 4
		NOR_D[12]			Nor flash data 12
		LDC_WD[14]			LDC Interface data 14
171	NF_D5	NF_D[5]	BI	4mA	NAND flash Interface data 5
		NOR_D[13]			Nor flash Interface Data 13
		LDC_WD[15]			LDC Interface WD 15
172	LDRD23	DISCHG	O	2mA	OTG charge pump Discharge
		NOR_WRB			Nor flash Interface WR
		LDC_WRB			LDC Interface WR
		LDR_D23			LDR Interface Data 23
		GPIOA14	BI		GPIOA Port 14
173	KSIN3	KS_IN[3]	BI	2mA	Key scan input 3
		GPIOA11	BI		GPIOA port 11
174	NF_D6	NF_D[6]	BI	4mA	NAND flash data 6
		NOR_D[14]			Nor flash interface data 14
		LDC_WD[16]			LDC Interface data 16
175	NF_D7	NF_D[7]	BI	4mA	NAND flash interface Data 7
		NOR_D[15]			Nor flash port data 15
		LDC_WD[17]			LDC Interface data 17
176	GND	GND	PWR	/	GND

27.2 ATJ2259B Pin Definition



ATJ2259B Pin Out

28 *Package Drawings*

28.1 ATJ2259B Package Drawing

Symbol	Dimension in mm			Dimension in Inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	0.12	0.16	0.004	0.005	0.006
D	21.60	22.00	22.40	0.850	0.866	0.882
D_1	—	20.00	—	—	0.787	—
E	21.60	22.00	22.40	0.850	0.866	0.882
E_1	—	20.00	—	—	0.787	—
e		0.40 BSC			0.016 BSC	
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1		1.00 REF			0.039 REF	
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	—	0.003	—	—
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ_1	0°	—	—	0°	—	—
θ_2	11°	12°	13°	11°	12°	13°
θ_3	11°	12°	13°	11°	12°	13°
ccc		0.08			0.003	

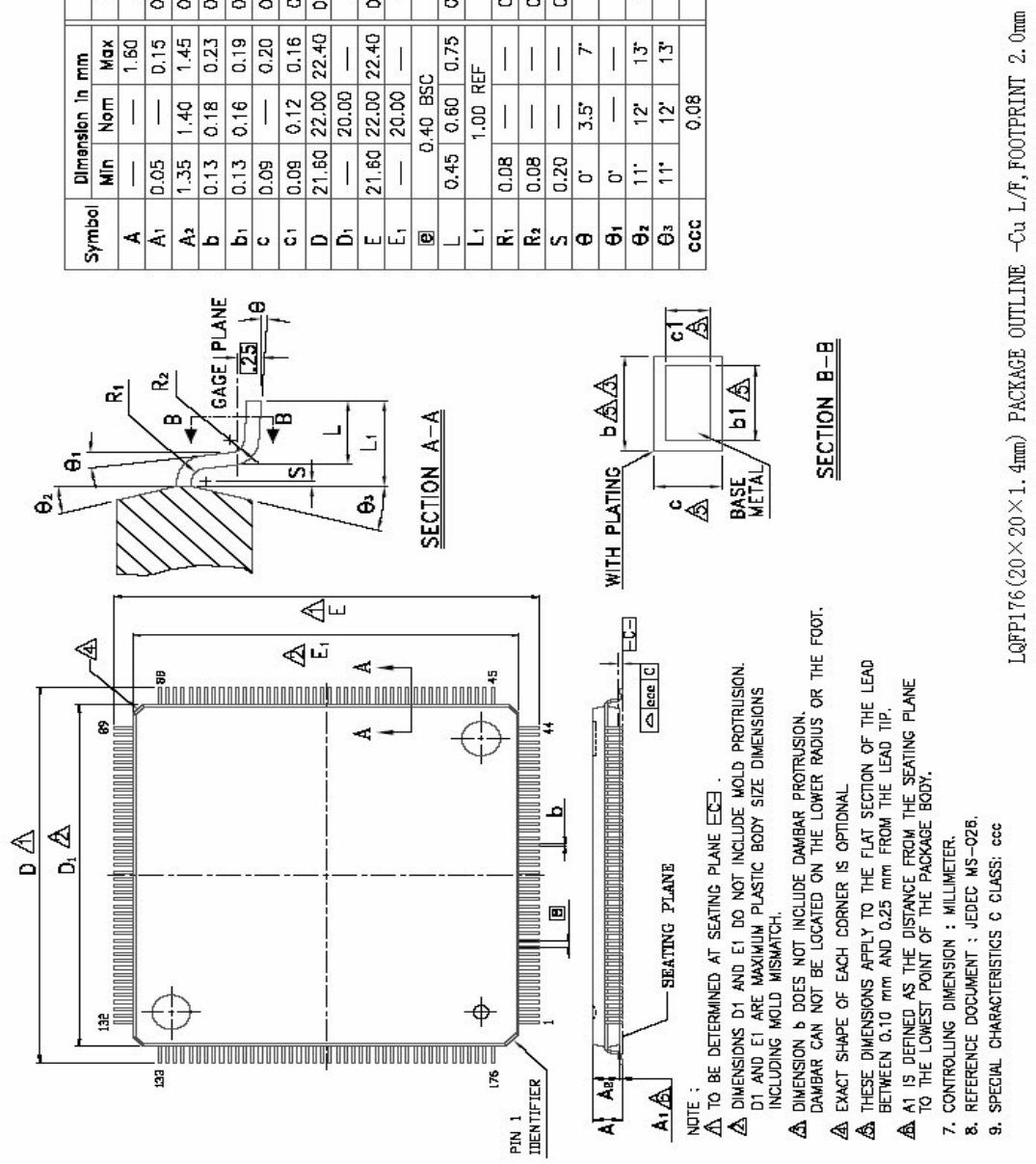


Figure: ATJ2259B Package Drawing

29 *Appendix*

29.1 Acronym and Abbreviations

ADC: Analog-to-Digital Converter
AHB: Advanced High-Performance Bus
ALE: Address-Locked Enable
APB: Advanced Peripheral Bus
BIST: Built-in Self-Test
CLE: Command-Locked Enable
CP0: System Control Coprocessor
CRC: Cyclic Redundancy Check
CVBS: Composite Video Broadcasting Signal
DAC: Digital-to-Analog Converter
dB: Decibel
DC: Direct Current
DSP: Digital Signal Processing
DVB: Digital Video Broadcasting
EAV: End of Active Video
ECC: Error Correct Code
FIR: Fast Infrared
GPIO: General-Purpose Input/Output
I2C: Inter-Integrated Circuit
I2S: Inter-IC Sound
IR: Infrared
IrDA: Infrared Data Association
IRQ: Interrupt Request
JPEG: Joint Photographic Experts Group
Li-Ion: Lithium Ion (battery type)
LRADC: Low Resolution ADC
MAC: Multiplier Accumulator Control
MIPS: Million Instructions per Second
MIR: Mid Infrared
MJPEG: Motion JPEG
MMC: Multimedia Card
MMU: Memory Management Unit

MLC: Multi-level Cell
MPEG: Motion Picture Expert Group
MS: Memory stick card
NTSC: National Television Standards Committee
OLED: Polymer Light-Emitting Diode
PA: Power Amplifier
PAL: Phase Alteration Line
PFM: Pulse Frequency Modulation
PLL: Phase-Locked Loop
PMU: Power Management Unit
PWM: Pulse Width Modulation
RISC: Reduced Instruction Set Computing
RTC: Real-Time Clock
SAV: Start of Active Video
SD: Secure Digital memory card
SIR: Slow Infrared
SMC: State Machine Controller
SLC: Single-Level Cell
SOC: System on a Chip
SPEC: Specification
SPI: Serial Peripheral Interface
SPRAM: Scratch Pad RAM
SW: Software
THD: Total Harmonic Distortion
TLB: Translation Look-aside Buffer
TS: Transport Stream
UART: Universal Asynchronous Receiver Transmitter
WMA: Windows Media Audio
WMV: Windows Media Video
LDC: CPU interface LCD

Actions Semiconductor Co., Ltd.
Address: Bldg.15-1, NO.1, HIT Rd., Tangjia, Zhuhai, Guangdong, China
Tel: +86-756-3392353
Fax: +86-756-3392251
Post Code: 519085
http://www.actions-semi.com
Business Email: mp-sales@actions-semi.com
Technical Service Email: mp-cs@actions-semi.com