



南方硅谷

Preliminary Data Sheet

SV6030P

Single-Chip 802.11 b/g/n MAC/BB/Radio with SDIO/SPI_SLAVE Interface

General Description

The SV6030P is a low-power single chip device providing for the highest level of integration for internet of thing embedded systems. It is designed to support all mandatory IEEE 802.11b data rates of 1, 2, 5.5 and 11 Mbps, all 802.11g payload data rates of 6, 9, 12, 18, 24, 36, 48 and 54 Mbps, as well as 802.11n MCS0~MCS7, 20MHz, 800ns and 400ns guard interval.

It includes a 2.4 GHz WLAN CMOS efficient power amplifier (PA) and an internal low noise amplifier (LNA). The Radio Frequency Front-end is single-ended bi-directional input and output.

The SV6030P has additional LDOs and DCDC buck convertor that could provide noise isolation for digital and analog supplies and excellent power efficient with minimum BOM cost.

The only external clock source needed for SV6030P based designs is a high speed crystal or oscillator. A variety of reference clocks are supported which include 19.2, 20, 24, 26, 38.4, 40 and 52 MHz

SV6030P Features

- All CMOS IEEE 802.11 b/g/n single chip
- Single stream 802.11n provides highest throughput and superior RF performance for embedded system
- Advanced 1x1 802.11n features:
 - Full / Half Guard Interval
 - Frame Aggregation
 - Reduced Inter-frame Space (RIFS)
 - Space Time Block Coding (STBC)
 - Greenfield mode
- Integrated WLAN CMOS efficient power amplifier with internal power detector and closed loop power calibration
- Supports interfaces by strapping option: SDIO 2.0 (50MHz, 4-bit) and SPI_SLAVE mode

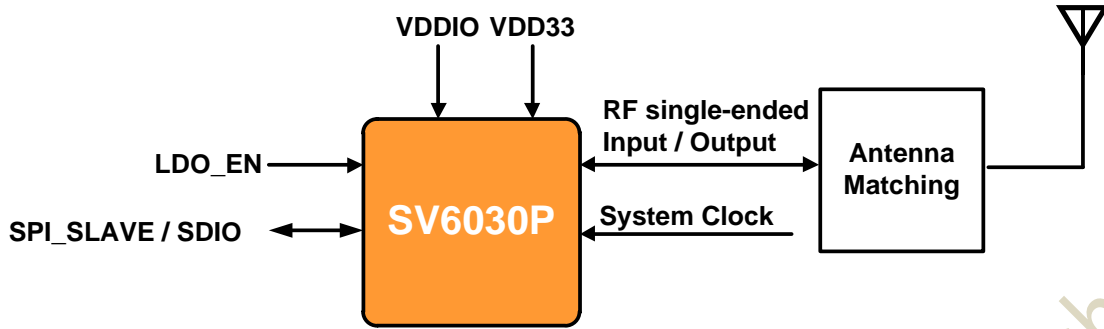
• ORDERING INFORMATION

Part Number	Package
SV6060P	Green/RoHS Compliant QFN 48L, 6x6 mm, 0.4mm pitch

All rights reserved

Proprietary and confidential information of iComm Corporation

October 2017



SV6030P System Block Diagram

iComm-semi Confidential Preliminary Datasheet

Liability Disclaimer

iComm Cooperation reserves the right to make changes without further notice to the product. IComm Cooperation does not assume any liability arising out of the application or use of any product or circuits described herein.

Revision History

Version	Date	Owner	Description
0.1	2015/09/18	Mason Wang	
0.2	2015/11/02	Mason Wang	
0.3	2016/08/11	Mason Wang	modify part no. from SSV6030P to SV6030P
0.4	2016/12/06	Mason Wang	Add table 7-2: Power Consumption at LDO mode (DCDC buck convertor is disable)
0.5	2017/10/11	Mason Wang	1, Update current consumption table 7-1 & table 7-2 2, Update table 4-6: Recommended Operating Conditions and DC Characteristics 3, Add section 4.2.1 Storage Condition 4, Add section 4.3 Thermal Characteristics

Table of Contents

1: System Overview.....	5
2: Power Supplies and Power Management.....	8
3: Interface Description.....	12
4: DC Characteristics.....	15
5: Frequency References.....	19
6: Electrical Specifications.....	20
7: System Power Consumption.....	22
8: Pin Descriptions.....	23
9: Package Information.....	27

1: SYSTEM OVERVIEW

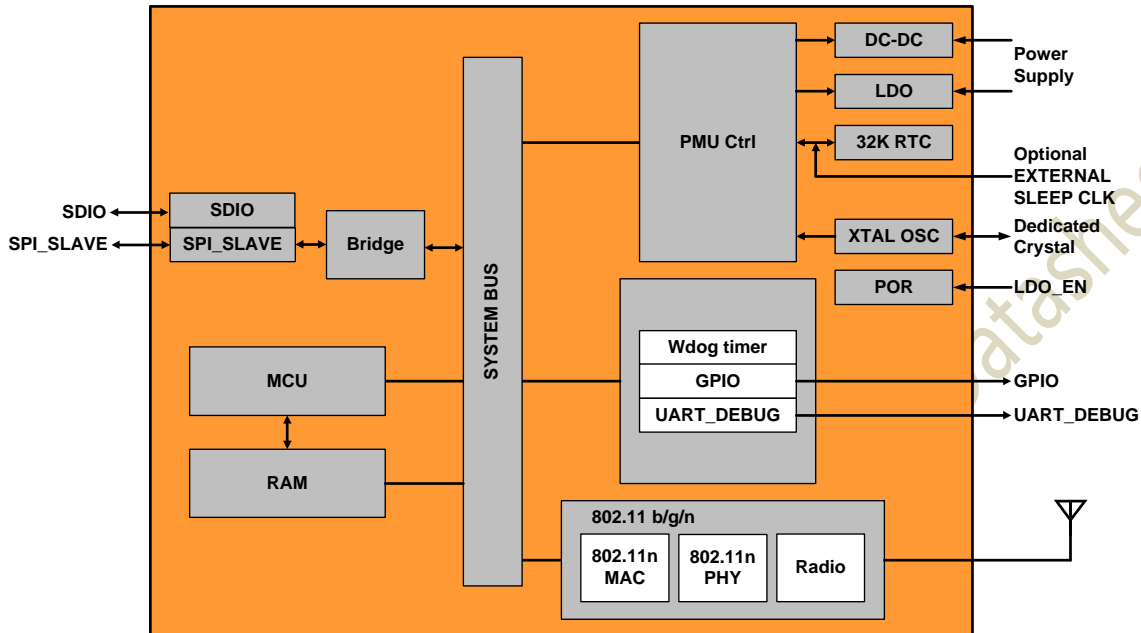


Figure 1-1: SV6030P Block Diagram

1.1 General Description

The SV6030P WLAN is designed to support IEEE 802.11 b/g/n single stream with the state-of-the-art design techniques and process technology to achieve low power consumption and high throughput performance to address the requirement of mobile and handheld devices. The SV6030P WLAN low power function uses the innovative design techniques and the optimized architecture which best utilizes the advanced process technology to reduce active and idle power, and achieve extreme low power consumption at sleep state to extend the battery life. The SV6030P WLAN A-MPDU Tx function maximizes the throughput performance while achieving the best buffer utilization.

1.2 MAC Features

- 802.11 b/g/n/e/i/d
- WLAN/BT coexistence mechanisms
- 802.11n features
 - A-MPDU Tx & Rx
 - Support immediate Block-Ack
- AP/STA mode
 - Soft-AP
- Rate adaption mechanism
- WFA features
 - WEP/TKIP/WPA/WPA2

- WMM/WMM PS
- WPS 1.0 and 2.0
- WiFi Direct(P2P)

1.3 PHY features

- 802.11b, 11g, and 802.11n 1T1R
- Short Guard Interval
- Greenfield mode
- RIFS in RX mode
- STBC in RX mode
- Enhanced and robust sensitivity for wider coverage range
- Supports calibration algorithm to handle no-idealities effects from CMOS RF block

1.4 CPU

- 32-bit micro-controller
- Support 192 KB Instruction SRAM with Data SRAM in total.

1.5 System BUS Blocks

The block acts as an arbiter. It has interfaces from two Masters:

- SPI_SLAVE,
- SDIO,
- CPU.

The data request can go into one of the three slaves: configuration space register blocks, packet buffers or internal Data SRAM depending on the address, the configuration space accesses can go to one of the places listed below:

- Radio
- GPIO
- UART_DEBUG
- MAC
- Digital Base Band

1.6 SPI_SLAVE

The SV6030P has a slave serial interface (SI) that can read/write command/status register and Tx/Rx data transaction, and be able to access directly external flash memory by relay mode, it has feature bellow,

- SPI to configuration space register accesses
- Support packet data Tx/Rx
- Support packet buffer, control/status register and SRAM access

1.7 GPIO

The SV6030P has 10 GPIO pins with direct software access. These GPIO pins are GPIO_8, GPIO_1, GPIO_2, GPIO_3, GPIO_5, GPIO_6, GPIO_15, GPIO_18, GPIO_19 and GPIO_20.

Many are multiplexed with other functions such as the host interface, UART_DEBUG, UART_DATA, I2C_MASTER, PWM_HW, etc. Each GPIO supports the following configurations via software programming:

- Internal weakly pull down option except that GPIO_5 has internal weakly pull up option
- Input available for sampling by a software register

1.8 System Clocking and Reset

The SV6030P has a system clocking block and reset which controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consist of clock enable and power signals which are used to gate the clocks going to internal modules. The system clocking and reset block also manages resets going to other modules within the device.

1.9 Design for Test

It also has features which enable testing of digital blocks via ATPG scan, memories via MBIST, analog components, and the radio.

iComm-semi Confidential Preliminary Datasheet

2: POWER SUPPLIES AND POWER MANAGEMENT

2.1 General Description and PMU Power Connection

The power management unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, Low Dropout Regulators (LDOs), buck DC-DC converter and reference bandgap circuit.

The PMU integrated multi-LDOs and one buck converter. Those circuits are optimized for the given functions by balancing quiescent current, dropout voltage, line / load regulation, ripple rejection and output noise.

The input voltage of the buck converter is 3.3V. Its output voltage is 1.6V and feeds into the input power of the RF circuit and DLDO which has 1.2V output voltage for all digital circuits.

There is only one PALDO for Tx PA, ANTSEL IO power with output voltage of 3.3V. There is also one dedicated LDO which provides 3.3V output voltage for RF blocks.

Figure 2-1 shows the typical power connection for SV6030P. DLDO and some RF circuits are powered by the buck converter output. The VDDIO is a power input which may be 1.8V, 2.5V or 3.3V from the host side. The connection structure is shown in the figure below.

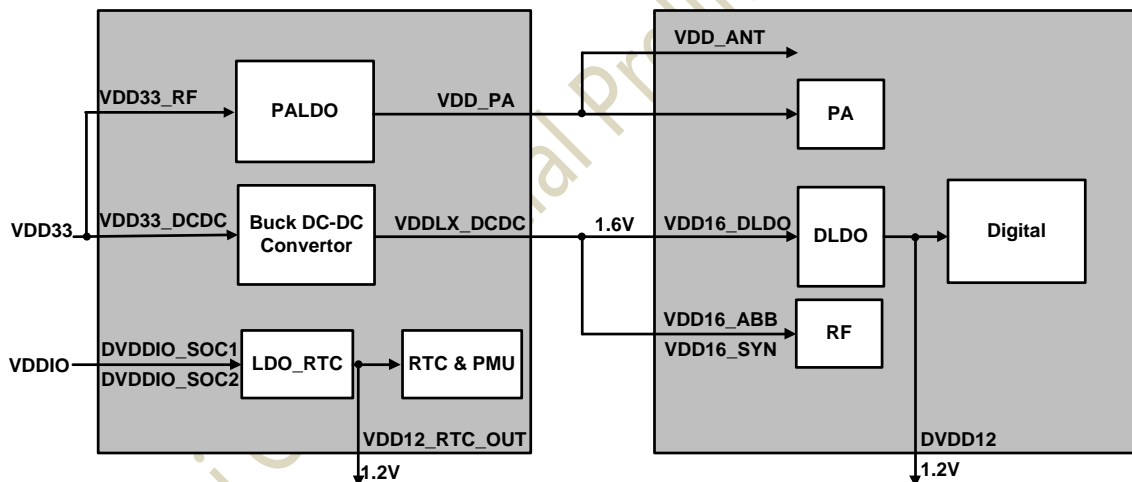


Figure 2-1: SV6030P Power Connection

2.2 Under-Voltage Lockout (UVLO)

The UVLO state in the PMU prevents startup if the initial voltage of the battery is below pre-defined threshold. It ensures that SV6030P is powered on with the battery in good condition. In addition, when the battery voltage is getting lower, it will enter the UVLO state, and the PMU will be turned off by itself to prevent further discharging.

2.3 PALDO

PA_LDO converts the supply input to a 3.3V supply for using WLAN transmitter circuits including PA. It is optimized for high-performance and adequate quiescent current.

2.4 DLDO

The DLDO is integrated in the PMU to supply digital core. It converts voltage from 1.6V input to 1.2V output which suits the digital circuits. The input is typically connected to the buck's output.

2.5 Buck Converter

The regulator is a DC-DC step-down converter (buck converter) to source 300mA (max.) with 2.0V to 1.5V programmable output voltage based on the register setting. It supplies power for the RF circuit and DLDO.

2.6 Power Management Control

There are three power modes that SV6030P operates when it is initialized: HOST_OFF, ACTIVE mode and SLEEP mode. There are two intermediate system transition modes: FW_DOWNLOAD and WARM_UP mode. The following are the brief introduction to each mode.

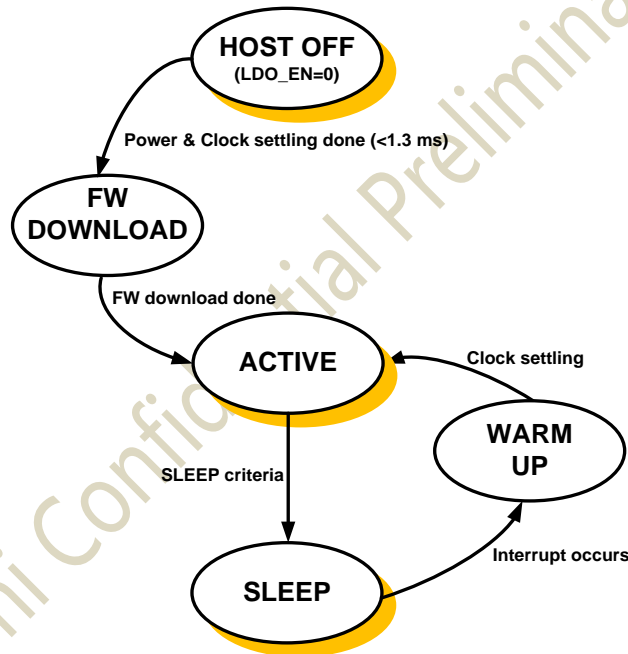


Figure 2-2: SV6030P Power State

Table 2-1: SV6030P Power State Description

State	Description
HOST OFF	When LDO_EN pin is de-asserted and logically low, the chip is brought to this state immediately.
	Sleep clock and internal power supply is disabled.
	After LDO_EN pin is asserted, the internal power and clock will be settled down within 1.3 ms.
FW DOWNLOAD	States for firmware download after power and clock is settled down.
SLEEP	The host controller can determine when to enter sleep to turn off most circuit in SV6030P. All the RF, DPLL circuits are turned off. In sleep mode, the system could be awakened after the sleep time is expired or by an external wake up signal from the host controller.
	All internal states are maintained and the Crystal oscillator is disabled.
WARM UP	The system transitions from SLEEP to ACTIVE. The crystal or oscillator is brought up and the PLL is enabled.
ACTIVE	The high speed clock is operational and sent to each block by the clock control register.
	The RF circuit is enabled to transmit or receive data, and the whole system is under normal operation.

2.7 Power-on Sequence

Figure 2-3 shows the power-on sequence of the SV6030P from power-up to firmware download, including the initial device power-on reset evoked by LDO_EN signal. The LDO_EN input level must be kept the same as VDDIO voltage level. After initial power-on, the LDO_EN signal can be held low to turn off the SV6030P or pulsed low to induce a subsequent reset. After LDO_EN is assert and host starts the power-on sequence of the SV6030P. From that point, the typical SV6030P power-on sequence is shown below:

1. Within 1.3 millisecond, the internal power-on reset (POR) will be done. And host could download firmware code of DPLL setting if the crystal is not default setting, 26MHz. The internal running clock is crystal frequency.
2. After 100us of DPLL settling time, host could set internal clock to full speed and finish all the downloading of firmware code.

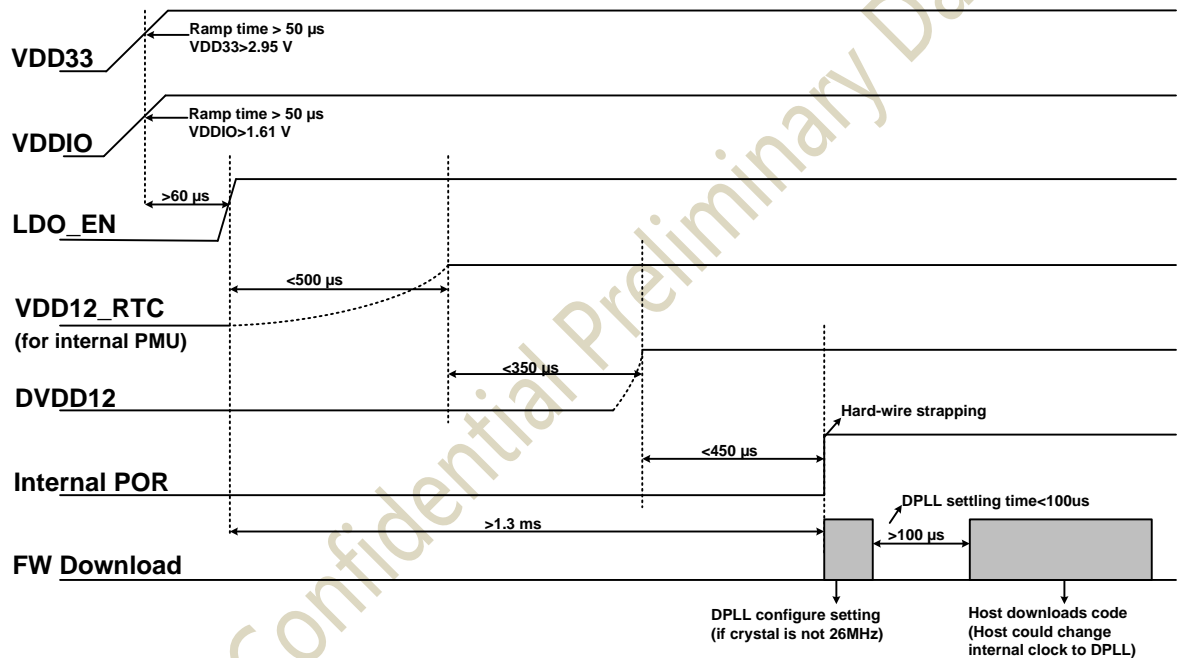


Figure 2-3: Power-on sequence

2.8 Reset Control

The SV6030P LDO_EN pin can be used to completely reset the entire chip. After this signal has been de-asserted, the SV6030P is in off mode waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules are held in reset. Once the host has initiated communication, the SV6030P turns on its crystal and later on DPLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

3: INTERFACE DESCRIPTION

3.1 SDIO Timing Waveform

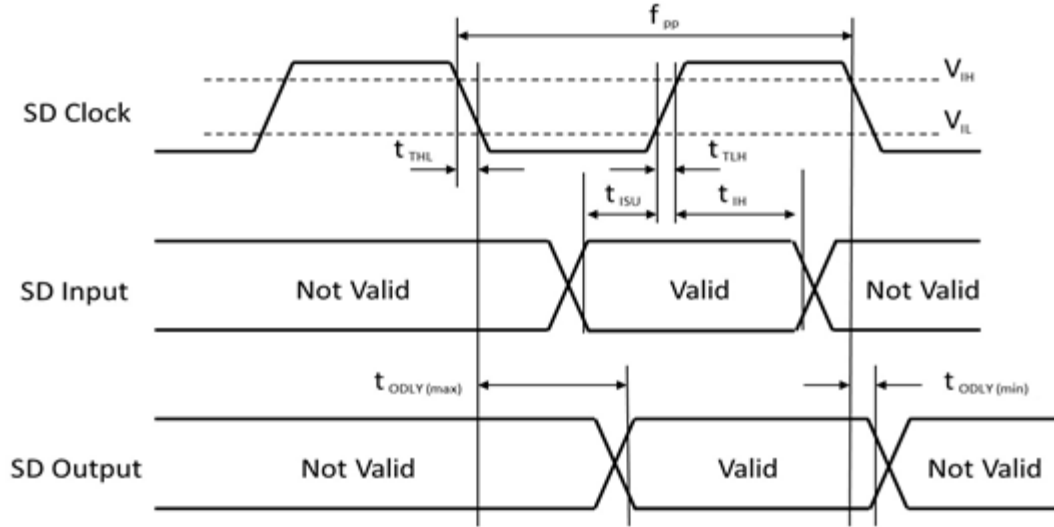
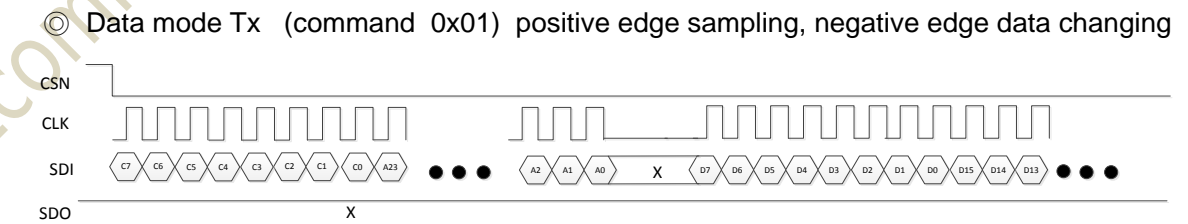
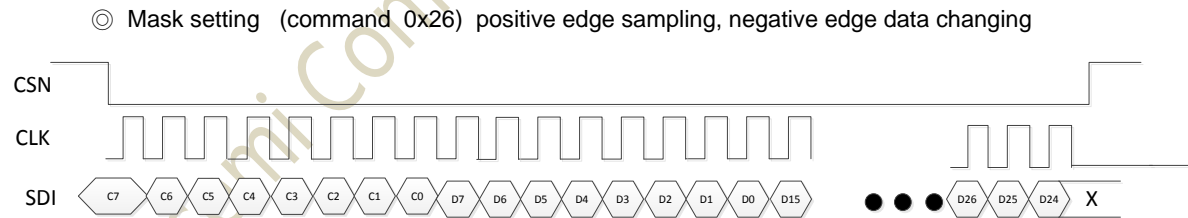
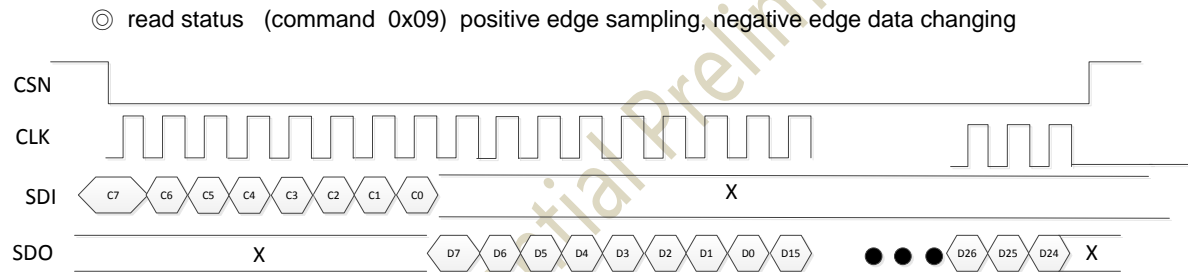
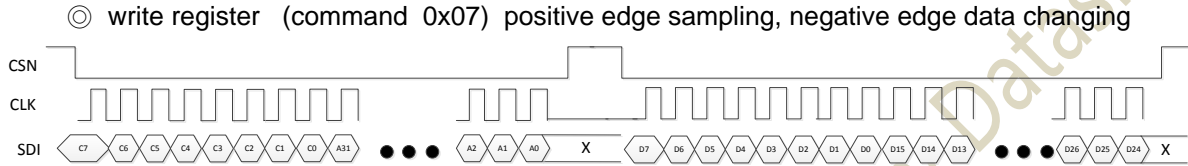
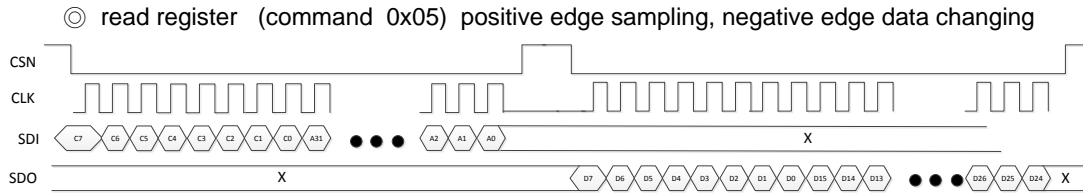


Table 3-1: SV6030P SDIO version 2.0 Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL}).					
f _{pp}	Clock frequency Data Transfer Mode	0		50	MHz
t _{TLH}	Clock rise time			3	ns
t _{THL}	Clock fall time			3	ns
Inputs CMD, DAT (reference to CLK)					
t _{ISU}	Input set-up time	6			ns
t _{IH}	Input hold time	2			ns
Outputs CMD, DAT (reference to CLK)					
t _{ODLY}	Output Delay time during Data Transfer Mode	4		9	ns

3.2 SPI_SLAVE Timing Waveform



© Data mode Rx (command 0x0C) positive edge sampling, positive edge data changing

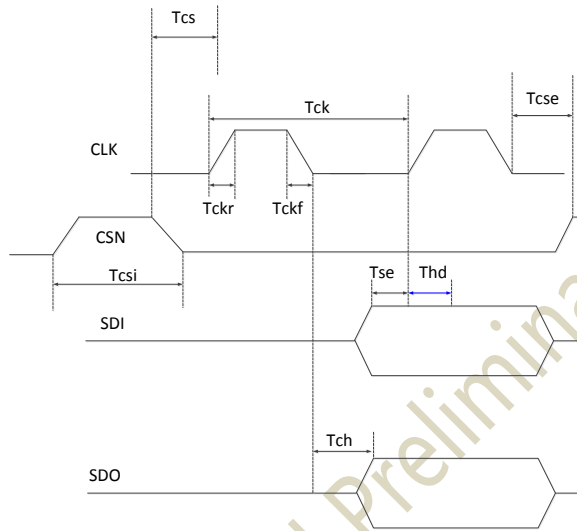
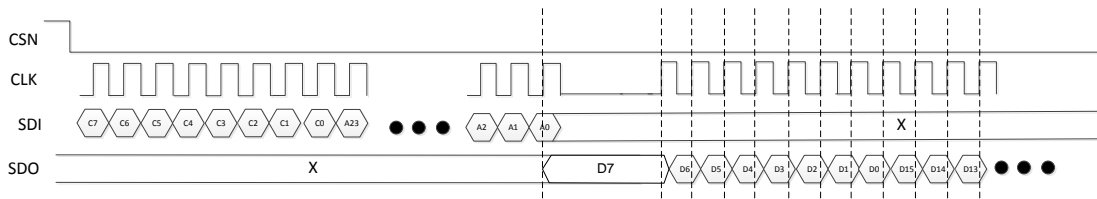


Table 3-2: SV6030P SPI_SLAVE Timing Specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
Tcs	Csn to clk post-edge time	300			ns
Tcsi	Time interval between tow csn edge	600			ns
Tck	Clk time	100			ns
Tckr	Clk rising time				ns
Tckf	Clk falling time				ns
Tse	Data input set up time				ns
Thd	Data input hold time				ns
Tch	Data output change time				ns
Tcse	Clk falling edge to csn time				ns

4: DC CHARACTERISTICS

4.1 Absolute Maximum Ratings

The absolute maximum ratings in Table 4-1 indicate levels where permanent damage to the device can occur, even if these limits are exceeded for only a brief duration. Functional operation is not guaranteed under these conditions. Operation at absolute maximum conditions for extended periods can adversely affect long-term reliability of the device.

Table 4-1: Absolute Maximum Ratings

Symbol (domain)	Description	Max Rating	Unit
VDD16_ABB	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD16_SYN	VDD input for analog 1.6V	-0.3 to 3.6	V
VDD_ANT	VDD input for external components I/O control	-0.3 to 3.6	V
EFUSE_VDD	VDD input for EFUSE burn-in. Pull low when read mode	-0.3 to 2.75	V
DVDDIO_SOC1	VDD input for GPIO pins	-0.3 to 3.6	V
DVDD12	VDD output for internal digital circuit	-0.3 to 1.32	V
VDD16_DLDO	VDD input for digital circuit	-0.3 to 3.6	V
VDD33_DCDC	VDD input for DCDC	-0.3 to 3.6	V
VDD12_RTC_OUT	VDD output for internal RTC circuit	-0.3 to 1.43	V
DVDDIO_SOC2	VDD input for GPIO pins (same level as DVDDIO_SOC1)	-0.3 to 3.6	V
VDD33_RF	VDD input for RF circuit	-0.3 to 3.6	V
VDD_PA	VDD output for internal PA	-0.3 to 3.6	V

4.2 Environmental Ratings

The environmental ratings are shown in Table 4-2

Table 4-2 Environmental Ratings

Characteristic	Conditions/Comments	Value	Units
Ambient Temperature (T_A)	Functional operation	-20 to +85	°C

4.2.1 Storage Condition

The calculated shelf life in sealed bag is 12 months if stored between 0°C and 40°C at less than 90% relative humidity (RH). After the bag is opened, devices that are subjected to solder reflow or other high temperature processes must be handled in the following manner:

- Mounted within 168-hours of factory conditions < 30 °C /60%RH
- Storage humidity needs to maintained at <10% RH

- c) Baking is necessary if customer exposes the component to air over 168 hrs, baking condition: 125°C / 8hrs

4.3 Thermal Characteristics

Table 4-3: the thermal characteristics of the SV6060P

Thermal characteristics without external heat sink in still air condition

Symbol	Description	Typ.	Unit
T _J	Maximum Junction Temperature (Plastic Package)	125	°C
θ _{JA}	Thermal Resistance θ _{JA} (°C/W) for JEDEC 4L system PCB	37.8	°C/W
θ _{JC}	Thermal Resistance θ _{JC} (°C/W) for JEDEC 4L system PCB	TBD	°C/W
Ψ _{Jt}	Thermal Characterization parameter Ψ _{Jt} (°C/W) for JEDEC 4L system PCB	4.13	°C/W
	Maximum Lead Temperature (Soldering 10s)	260	°C

Notes: * JEDEC 51-7 system FR4 PCB size: 3" x 4.5" (76.2 x 114.3 mm)

* Thermal characteristics without external heat sink in still air condition

4.4 PMU Under Voltage Lock-out (UVLO) Characteristics

Table 4-4 PMU UVLO characteristics

Symbol (domain)	Description	Min.	Typ.	Max.	Unit
Under Voltage Lock-Out (UVLO)					
Under voltage rising threshold of VBAT	VDD33: pin VDD33_DCDC & VDD33_RF		2.95		V
Under voltage falling threshold of VBAT	VDD33: pin VDD33_DCDC & VDD33_RF		2.85		V
Under voltage rising threshold of DVDDIO	DVDDIO: pin DVDDIO_SOC1 & DVDDIO_SOC2		1.6		V
Under voltage falling threshold of DVDDIO	DVDDIO: pin DVDDIO_SOC1 & DVDDIO_SOC2		1.5		V

4.5 Electrostatic Discharge Specifications

This is an ESD sensitive product! Observe precaution and handle with care. Extreme caution must be exercised to prevent electrostatic discharge (ESD) damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices.

Table 4-5: ESD Specifications

Pin Type	Test Condition	ESD Rating	Unit
Human Body Mode (HBM)	refers to MIL-STD-883G Method 3015.7	Pass ± 2.5	KV
Machine Mode (MM)	refers to JEDEC EIA/JESD22-A115	Pass ± 250	V

4.6 Recommended Operating Conditions and DC Characteristics

Table 4-6: Recommended Operating Conditions and DC Characteristics

Domain (Symbol)	Description	Min.	Typ.	Max.	Unit
VDD16_ABB	VDD input for analog 1.6V		1.6		V
VDD16_SYN	VDD input for analog 1.6V		1.6		V
VDD_ANT	VDD input for external components I/O control	3.13	3.3	3.46	V
EFUSE_VDD	VDD input for EFUSE burn-in. Pull low when read mode	2.25	2.5	2.75	V
DVDDIO_SOC1	VDD input for GPIO pins	1.71	1.8/2.5/3.3	3.46	V
DVDD12	VDD output for internal digital circuit		1.2		V
VDD16_DLDO	VDD input for digital circuit's LDO		1.6		V
VDD33_DCDC	VDD input for DCDC	3.13	3.3	3.46	V
VDD12_RTC_OUT	VDD output for internal RTC circuit		1.3		V
DVDDIO_SOC2	VDD input for GPIO pins (same level as DVDDIO_SOC1)	1.71	1.8/2.5/3.3	3.46	V
VDD33_RF	VDD input for RF circuit	3.13	3.3	3.46	V
VDD_PA	VDD output for internal PA	3.13	3.3	3.46	V
(V _{IL})	Input Low voltage when VDDIO=3.3V	-0.3		0.8	V
(V _{IH})	Input High voltage when VDDIO=3.3V	2		3.6	V
(V _{T+})	Schmitt trigger low to high threshold voltage when VDDIO=3.3V	1.6	1.74	1.89	V
(V _{T-})	Schmitt trigger high to low threshold voltage when VDDIO=3.3V	1.27	1.4	1.56	V
(V _{OL})	Output low voltage when VDDIO=3.3V			0.4	V
(V _{OH})	Output high voltage when VDDIO=3.3V	2.4			V

(R_{PD})	Input weakly pull-down resistance when VDDIO=3.3V. All GPIO pins have internal weakly pull-down option except that GPIO_5 has internal weakly pull-up option	35	51	84	K Ω
(R_{PU})	Input weakly pull-high resistance when VDDIO=3.3V. Only GPIO_5 has internal weakly pull-up option	35	51	84	K Ω
(I_{OL})	Low level output current @ V _{OL} (max), 8mA setting	11.9	17.7	23.4	mA
	Low level output current @ V _{OL} (max), 12mA setting	15.8	23.5	31.1	mA
(I_{OH})	High level output current @ V _{OH} (min), 8mA setting	17.2	34.1	58.8	mA
	High level output current @ V _{OH} (min), 12mA setting	23.9	47.2	81.5	mA

5: FREQUENCY REFERENCES

5.1 Crystal Oscillator Specifications

Table 5-1: Crystal Oscillator Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
Crystal load Capacitance	–	–	10		pF
ESR	–	–	–	70	Ω
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm

5.2 External Clock-Requirements and Performance

Table 5-1: External Clock-Requirements and Performance

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range	–	Between 19.2MHz~52MHz			
OSCIN Input Voltage	AC-couple analog signal	400	–	1500	mV _{PP}
Frequency tolerance Initial and over temperature	–	-20ppm	–	20ppm	ppm
Duty Cycle	26MHz clock	40	50	60	%
Phase Noise (802.11b/g)	26MHz clock at 1KHz offset	–	–	-119	dBc/Hz
	26MHz clock at 10KHz offset	–	–	-129	dBc/Hz
	26MHz clock at 100KHz offset	–	–	-134	dBc/Hz
	26MHz clock at 1MHz offset	–	–	-139	dBc/Hz
Phase Noise (802.11n 2.4GHz)	26MHz clock at 1KHz offset	–	–	-125	dBc/Hz
	26MHz clock at 10KHz offset	–	–	-135	dBc/Hz
	26MHz clock at 100KHz offset	–	–	-140	dBc/Hz
	26MHz clock at 1MHz offset	–	–	-145	dBc/Hz

6: Electrical Specifications

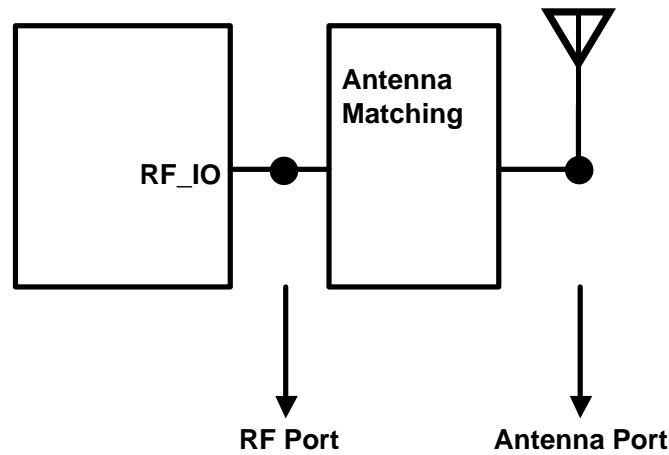


Figure 6-1: RF Front-End Reference Topology for RF Performance

Note: All specifications are measured at the Antenna Port unless otherwise specified.

6.1 WLAN RF Performance Specifications

Table 6-1: WLAN RF Performance Specifications

Parameter	Condition/Notes	Min.	Typ.	Max.	Unit
Frequency Range		2412	-	2484	MHz
Rx Sensitivity (CCK)	CCK, 1 Mbps		-95.5		dBm
	CCK, 2 Mbps		-93.5		dBm
	CCK, 5.5 Mbps		-91.0		dBm
	CCK, 11 Mbps		-88.0		dBm
Rx Sensitivity (OFDM)	OFDM, 6 Mbps		-91.5		dBm
	OFDM, 9 Mbps		-90.0		dBm
	OFDM, 12 Mbps		-88.0		dBm
	OFDM, 18 Mbps		-86.0		dBm
	OFDM, 24 Mbps		-82.5		dBm
	OFDM, 36 Mbps		-79.5		dBm
	OFDM, 48 Mbps		-74.5		dBm
	OFDM, 54 Mbps		-73.5		dBm
Rx Sensitivity (HT20) Greenfield 800nS GI Non-STBC	HT20, MCS0		-91.0		dBm
	HT20, MCS1		-88.0		dBm
	HT20, MCS2		-86.0		dBm
	HT20, MCS3		-81.5		dBm
	HT20, MCS4		-79.0		dBm
	HT20, MCS5		-74.5		dBm
	HT20, MCS6		-73.5		dBm
	HT20, MCS7		-72.5		dBm

RX Adjacent Channel Rejection (CCK)	CCK, 1 Mbps (30 MHz offset)		41		dB
	CCK, 11 Mbps (25 MHz offset)		41		dB
RX Adjacent Channel Rejection (OFDM)	OFDM, 6 Mbps (25 MHz offset)		39		dB
	OFDM, 54 Mbps (25 MHz offset)		23		dB
RX Adjacent Channel Rejection (HT20)	HT20, MCS0 (25 MHz offset)		38		dB
	HT20, MCS7 (25 MHz offset)		21		dB
TX Output Power	CCK, 1-11 Mbps		19		dBm
	OFDM, 54 Mbps		16		dBm
	HT20, MCS7		15		dBm

Icomm-semi Confidential Preliminary Datasheet

7: System Power Consumption

Note: All results are measured at the condition that VIO and VBAT are 3.3V.

Table 7-1: Power Consumption at DCDC mode (DCDC buck convertor is enable)

WLAN Operational Modes	Typ.	Unit
OFF ^a	4	uA
Rx, CCK, 1 Mbps	60	mA
Rx, OFDM, 54 Mbps	66	mA
Rx, HT20, MCS7	67	mA
Sleep	200	uA
Rx Power Saving, DTIM= 1	1.9	mA
Tx, CCK, 1 Mbps	282	mA
Tx, OFDM, 54 Mbps	218	mA
Tx, HT20, MCS7	223	mA

Table 7-2: Power Consumption at LDO mode (DCDC buck convertor is disable)

WLAN Operational Modes	Typ.	Unit
OFF ^a	4	uA
Rx, CCK, 1 Mbps	91	mA
Rx, OFDM, 54 Mbps	101	mA
Rx, HT20, MCS7	103	mA
Rx Power Saving, DTIM= 1	2.4	mA
Tx, CCK, 1 Mbps	290	mA
Tx, OFDM, 54 Mbps	237	mA
Tx, HT20, MCS7	239	mA

- a. OFF mode test condition: VBAT=3.3V, VIO=3.3V, LDO_EN=0V. Pin 43 "VDD_PA" is output pin with decoupling capacitor and not tied to VBAT.

8: Pin Descriptions

This section contains a listing of the signal descriptions (see Figure 8-1 for the SV6030P QFN package pin-out)

The following nomenclature is used for signal names:

NC	No connection should be made to this pin
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name, indicates the negative side of a differential signal

The following nomenclature is used for signal types described in Table 6-1:

IA	Analog input signal
I	Digital input signal
IO	Digital bidirectional signal
IOA	Analog bidirectional signal
O	Digital output signal
P	Power signal
G	Ground signal

Table 8-1: SV6030P Package Pin-out

No.	Name	Description	Type (default)
1	NC	No connection	NC
2	NC	No connection	NC
3	VDD16_ABB	Analog 1.6V supply	P
4	VDD16_SYN	Analog 1.6V supply	P
5	WIFI_TX_SW	Control signal for external WiFi Tx switch or WiFi switch (WIFI_SW)	I
6	WIFI_RX_SW	Control signal for external WiFi Rx switch	I
7	BT_SW	Control signal for external BT switch	I
8	VDD_ANT	External components control I/O supply	P
9	XTALP	Crystal input	IA
10	XTALN	Crystal input or external reference clock input	IA
11	EFUSE_VDD	EFUSE burn-in supply	P
12	NC	No connection	NC
13	NC	No connection	NC
14	GPIO_8	GPIO pin and strapping_pin_1	O
15	DVDDIO_SOC1	SOC1 GPIO I/O supply	P
16	GPIO_1	GPIO pin and strapping_pin_2	O
17	DVDD12	Digital 1.2V supply	P
18	GPIO_2		I
19	GPIO_3		I
20	VDD16_DLDO	Digital 1.6V supply	P
21	VDD33_DCDC	DCDC 3.3V supply	P
22	VDDLX_DCDC	Buck converter feedback	P
23	VDD16_DCDC_OUT	Buck converter 1.6V output	P
24	NC	No connection	NC
25	NC	No connection	NC
26	LDO_EN	Reset signal to power down the SV6030P	I
27	VDD12_RTC_OUT	RTC 1.2V supply	P
28	DVDDIO_SOC2	SOC2 GPIO I/O supply	P
29	GPIO_9	SDIO command / SPI_SLAVE_mosi	
30	GPIO_10	SDIO data pin bit 3 / SPI_SLAVE_CSN	
31	GPIO_11	SDIO data pin bit 2	
32	GPIO_12	SDIO data pin bit 1 / SPI_SLAVE host interrupt	
33	GPIO_13	SDIO data pin bit 0 / SPI_SLAVE_miso	
34	GPIO_14	SDIO clock / SPI_SLAVE_SCLK	
35	GPIO_5		I
36	DVDD12	Digital 1.2V supply	P
37	GPIO_6		I
38	GPIO_15		O
39	GPIO_18		O
40	GPIO_19		I
41	GPIO_20	GPIO pin and strapping_pin_3	O

42	VDD33_RF	RF 3.3V supply	P
43	VDD_PA	PA supply	P
44	NC	No connection	NC
45	RF_IO	2.4 GHz RF input & output port	IOA
46	NC	No connection	NC
47	NC	No connection	NC
48	NC	No connection	NC

Table 8-2 shows the strapping option controlled by strapping pins. The strapping value will be set after power-on reset and the HOST controlled interface will be determined. The strapping pins (strapping_pin_3, strapping_pin_2 and strapping_pin_1) are corresponding to GPIO pins: GPIO_20, GPIO_1 & GPIO_8. Host controlled interface option are selection by the strapping pins. No need of strapping resistor for pull down strapping value. The strapping high voltage must be the same as VIO voltage.

Table 8-2: SV6030P Strapping Pin Table

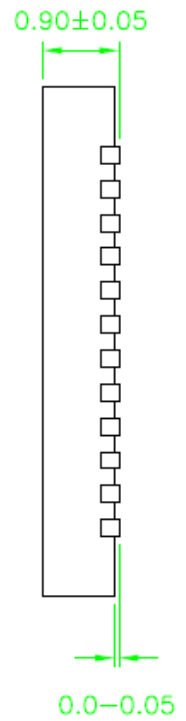
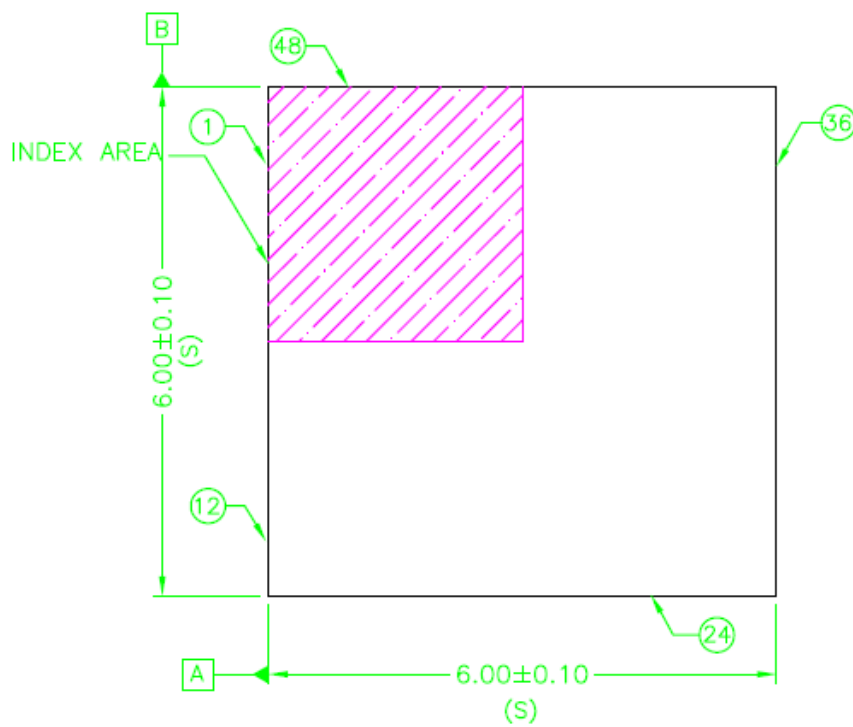
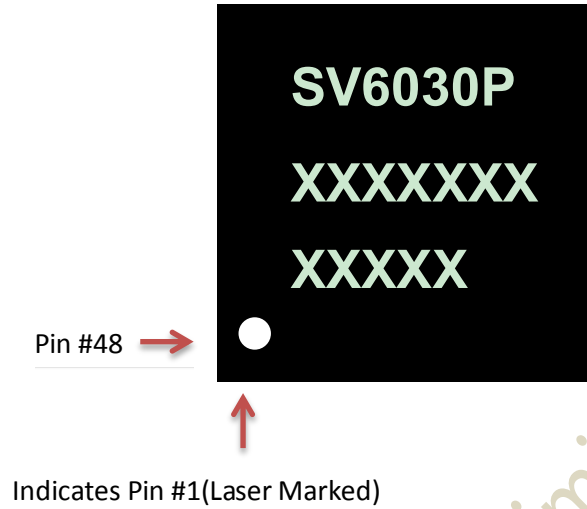
Strapping_pin_3, strapping_pin_2 & strapping_pin_1 (GPIO_20, GPIO_1 & GPIO_8)	Typ.
000 (Default, no external strapping resistor needed)	SDIO 2.0, 4 bit
001	SPI_SLAVE mode
Other values	Forbidden

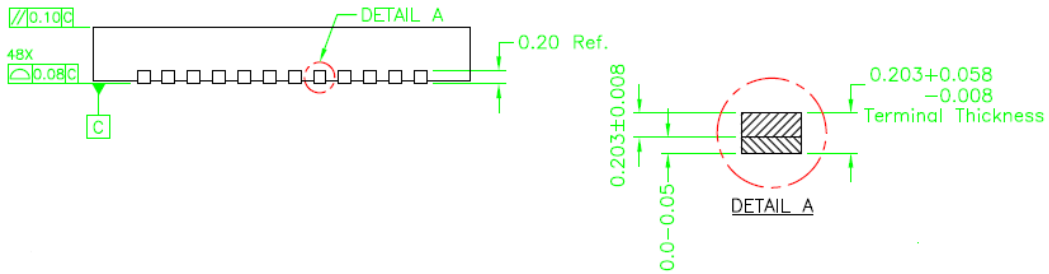
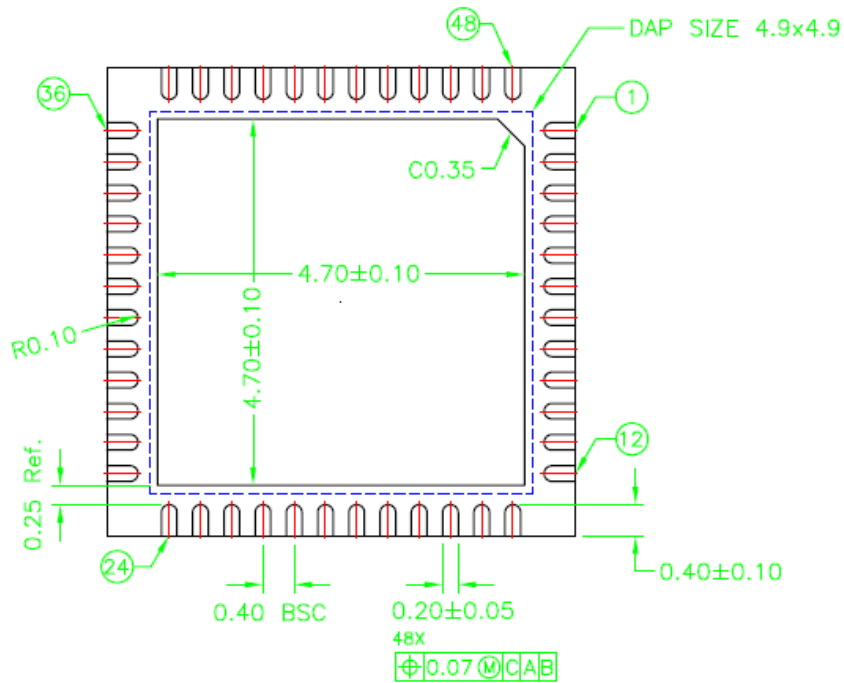
*Note: Pull-up strapping resistor value ~ 20 Kohm

9: PACKAGE INFORMATION

6 x 6 mm (body size), 0.4mm pitch QFN-48

Marking format (top view)





NOTE :

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH / PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC. (S)
5. L/F STOCK# FR9012 (PPF)

Figure 9-1: SV6030P QFN 6 x 6 mm Package Dimensions